Course code	Course Name	L-T-P - Credits	Year of Introduction
EE365	Digital System Design	3-0-0-3	2016

Prerequisite: Nil

Course Objectives

- To enable designing and building of real digital circuits
- To implement VHDL programming in digital system design

Syllabus

Combinational logic using VHDL gate models, Combinational building blocks, Synchronous Sequential Design, VHDL Models of Sequential Logic Blocks, Complex Sequential Systems, VHDL Simulation, VHDL Synthesis, Testing Digital Systems, Design for Testability.

Expected outcome.

After completing the course, the students will be able to

i. Design any Digital Circuit for practical application
ii. Implement any digital system using VHDL
iii. Program any VHDL code for practical implementation
iv. Hardware realization of any complex VHDL system.

Text Book:

Mark Zwolinski, Digital System Design with VHDL, Second Edition, Pearson Education.2007

References:

1. A Anandakumar, Digital Electronics,Prentice Hall India Feb 2009.
2. John F Wakerly, Digital Design, Pearson Education, Delhi, 2002
3. Morris Mano,Digital Design, Pearson Education, Delhi, 2002

Course Plan

Module	Contents	Hours	Sem. Exam Marks
I	Introduction : Modern Digital Design, CMOS Technology, Programmable Logic ,Electrical Properties Combinational Logic Design : Boolean Algebra , Logic Gates, Combinational Logic Design, Timing, Number codes	4	15%
II	Combinational Logic using VHDL Gate Models : Entities and Architectures ,Identifiers , Spaces and Comments ,Net lists , Signal Assignments ,Generics ,Constant and Open Ports ,Test benches, Configurations Combinational Building Blocks : Three-Stat Buffers , Decoders ,Multiplexers, Priority Encoders , Adders, Parity Checkers , Test benches for Combinational blocks	8	15%
FIRST INTERNAL EXAMINATION			
III	Synchronous Sequential Design : Synchronous Sequential Systems , Models of Synchronous Sequential Systems, Algorithmic State Machines ,Synthesis from ASM chart , State Machines in VHDL , VHDL Test benches for State Machines	7	15%

IV	VHDL Models of Sequential Logic Blocks : Latches , Flip-Flops , J K and T Flip Flop , Registers and Shift Registers ,Counters , Memory, Sequential Multiplier, Test benches for Sequential Building Blocks Complex Sequential Systems : Data path / Control Partitioning ,Instructions, A Simple Microprocessor, VHDL model of a Simple Microprocessor	8	15%
SECOND INTERNAL EXAMINATION			
V	VHDL Simulation: Event Driven Simulation, Simulation of VHDL models , Simulation modelling issues , Fire Operations . VHDL Synthesis : RTL Synthesis , Constraints ,Synthesis for FPGAs ,Behavioural Synthesis , Verifying Synthesis Results	8	20%
VI	Testing Digital Systems : Need for Testing , Fault Models , Fault oriented Test Pattern Generation , Fault Simulation, Fault Simulation in VHDL Design for Testability : Ad Hoc Testability improvements , Structured Design for Test , Built-in-Self-Test , Boundary scan (IEEE 1149 .1)	7	20%
END SEMESTER EXAM			

QUESTION PAPER PATTERN:

Maximum Marks: 100 Exam Duration: 3Hourrs.

Part A: 8 compulsory questions.

One question from each module of Module I - IV; and two each from Module V & VI.

Student has to answer all questions. (8 x5)=40

Part B: 3 questions uniformly covering Modules I & II. Student has to answer any 2 from the 3 questions: (2 x 10) =20. Each question can have maximum of 4 sub questions (a,b,c,d), if needed.

Part C: 3 questions uniformly covering Modules III & IV. Student has to answer any 2 from the 3 questions: (2 x 10) =20. Each question can have maximum of 4 sub questions (a,b,c,d), if needed.

Part D: 3 questions uniformly covering Modules V & VI. Student has to answer any 2 from the 3 questions: (2 x 10) =20. Each question can have maximum of 4 sub questions (a,b,c,d), if needed.