Department of Electrical Engineering

College of Engineering Trivandrum

Lab Manual

ELECTRONIC CIRCUITS LAB

Course: **PCEEL308 ANALOG ELECTRONICS LAB**

Department of Electrical Engineering

College of Engineering Trivandrum

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Vision

Be a centre of excellence and higher learning in Electrical Engineering and allied areas.

Mission

- To impart quality education in Electrical Engineering and bring-up professionally competent engineers.
- To mould ethically sound and socially responsible Electrical Engineers with leadership qualities.
- To inculcate research attitude among students and encourage them to pursue higher studies.

Program Educational Objectives (PEOs)

Graduates will

1. excel as technically competent electrical engineers.
2. excel in higher studies and build on fundamental knowledge to develop technical skills within and across disciplines.
3. have the ability to function effectively as members or leaders in technical teams.
4. adapt to changes in global technological scenario and societal needs through lifelong learning

Programme Outcomes

1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. Individual and teamwork: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes

1. Apply engineering knowledge to analyse, model, design and operate modern systems for generation, transmission, distribution and control of electrical power.

2. Design, develop and test modern hardware and software systems for signal processing, measurement, instrumentation and control applications.

PCEEL308 – ANALOG ELECTRONICS LAB

Course Outcomes

CO 1 - Use the various electronic instruments and for conducting experiments. (K1)

CO 2 - Design and develop various electronic circuits using diodes and Zener diodes. (K3)

CO 3 - Design and implement amplifier and oscillator circuits using BJT and JFET. (K3)

CO 4 - Design and implement basic circuits using IC (OPAMP and 555 timers). (K3)

CO 5 - Simulate electronic circuits using any circuit simulation software. (K3)

CO6 - Use PCB layout software for circuit design. (K2)

DEPARTMENT OF ELECTRICAL ENGINEERING

ELECTRONICS CIRCUITS LAB

PCEEL308 – ANALOG ELECTRONICS LAB
Cycle of Experiments

Pre-Lab Assignment: Familiarization of CRO and Function Generator

: Introduction to circuit simulation using any circuit simulation software.

Cycle 1

1. Clipping and Clamping Circuits 2
2. Simple Zener Regulator 6
3. Common Emitter Amplifier 9

Cycle 2

4. Integrator and Differentiator Using Op-Amp 13
5. Inverting and Non-Inverting Amplifier Using Op-Amp 16
6. Series Voltage Regulator 19

Cycle 3

7. Precision Rectifier using Op-Amp 30
8. Astable And Monostable Multivibrator Using IC555 32
9. RC Phase Shift Oscillator Using BJT 35

Cycle 4

10. Wien Bridge Oscillator Using Op-Amp 37
11. Waveform Generator Using Op-Amp 41
12. Comparator and Schmitt Trigger Circuit Using Op-Amp 45

Cycle 5

13. MOSFET Amplifier 48
14. Basic RC circuits- High pass and Low pass filters 51
15. Introduction to PCB layout software. 55

Pre-Lab Assignment-2

Introduction to circuit simulation using any circuit simulation software.

LTspice is a free and powerful circuit simulation software, developed by Analog Devices, that allows users to design, analyze, and troubleshoot electronic circuits before physical implementation. It's a SPICE-based simulator, meaning it uses mathematical models to emulate the behavior of electronic components and circuits.

Aim: To perform circuit simulation using LTspice.

Link to download software and tutorials

https://www.analog.com/en/resources/design-tools-and-calculators/ltspice-simulator.html

Experiment No. 1

CLIPPING AND CLAMPING CIRCUITS

AIM

To realise different clipping and clamping circuits and observe the waveforms.

THEORY

Clipping Circuits

Clipping circuits are nonlinear wave shaping circuits. A clipping circuit is useful to cut off the positive or negative portions of an input waveform. Clipping circuits are also known as voltage limiters or slicers.

Positive clipper

The positive half cycle is clipped by diode and only the drop across diode will appear across the load. During negative half cycle, the diode does not conduct and the voltage across R_L is given by

$$V_L = V_S \frac{R_L}{R_L + R}$$

Since $R_L >> R$, the output voltage will be close to input voltage during negative half cycle.

Negative clipper

The negative half cycle is clipped by diode and only the drop across diode will appear across the load. During positive half cycle, the diode does not conduct and the voltage across R_L is given by

$$V_L = V_S \frac{R_L}{R_L + R}$$

Since $R_L >> R$, the output voltage will be close to input voltage during the positive half cycle.

Biased positive clipper

Here a reference voltage is given to the clipper circuit by a zener diode. Up to V_z, the output voltage is

$$V_0 = V_{in}\, R_L /(R_L+R)$$

At $V_o = V_z$, the zener breakdown occurs and the voltage V_o is constant. Here the reference voltage is used to clip only a part of the positive half cycle.

Biased negative clipper

The principle is similar to that of a biased positive clipper. Here a reference voltage is provided by a zener diode to clip a portion of the negative half cycle. During the positive half cycle

$$V_0 = V_{in}\, R_L/(R_L+R)$$

Slicer

This is the combination of both biased positive clipper and biased negative clipper. The peak portion of the signal determined by the zener voltage reference is clipped.

Clamping Circuit

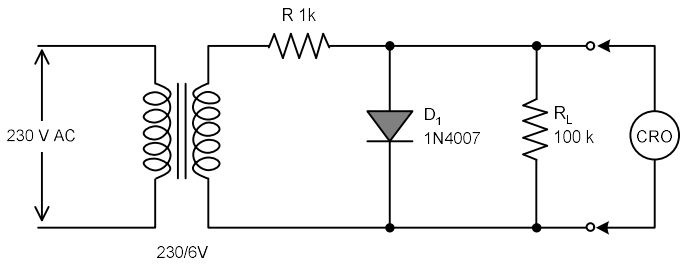
Clamping is a function which must be frequently performed with a periodic waveform in the establishment of the recurrent positive or negative extremity at some constant reference level. Clamping circuits are also referred to as dc restorer or dc inserter.

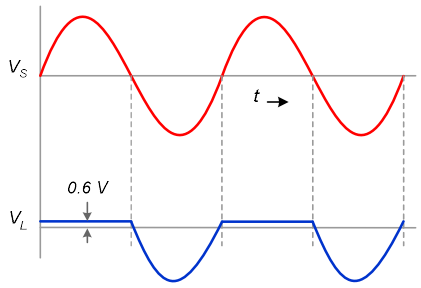
A positive clamper adds positive dc level and a negative clamper adds a negative dc level. A positive clamper clamps a negative extremity of the input signal to the reference voltage level. A negative clamper adds to negative dc level by clamping the positive extremity of the input to the reference voltage level.

PROCEDURE

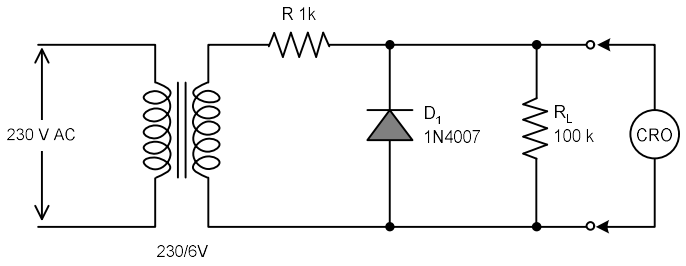
The circuits are wired as in the circuit diagram. Connect the input terminals to 230V ac supply and the output terminals to a CRO.

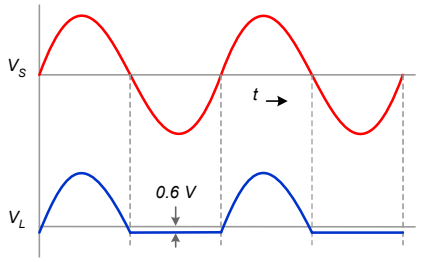
Positive clipper



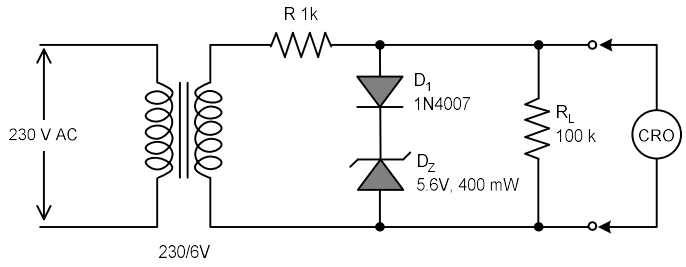


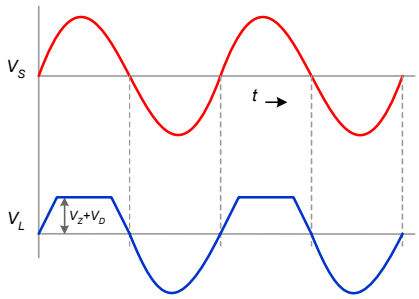
Negative clipper



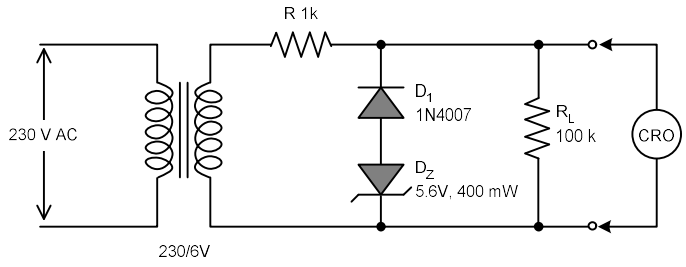


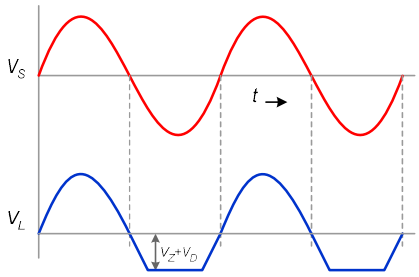
Biased Positive clipper



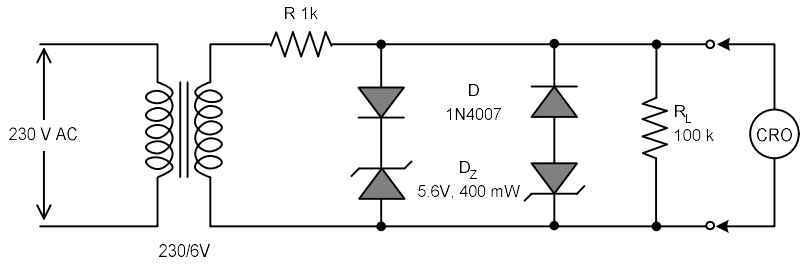


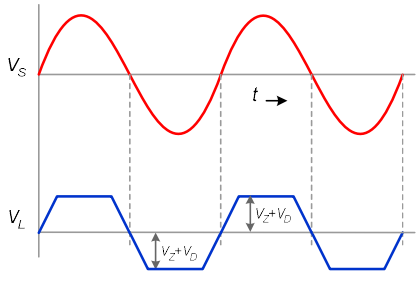
Biased Negative clipper



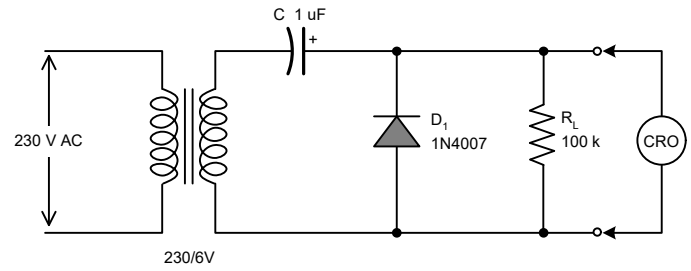


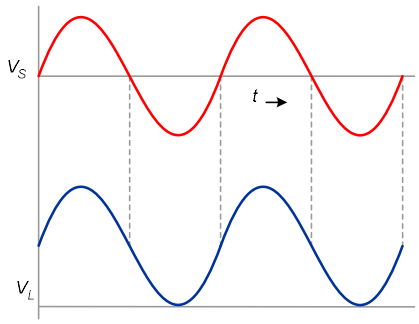
Slicer



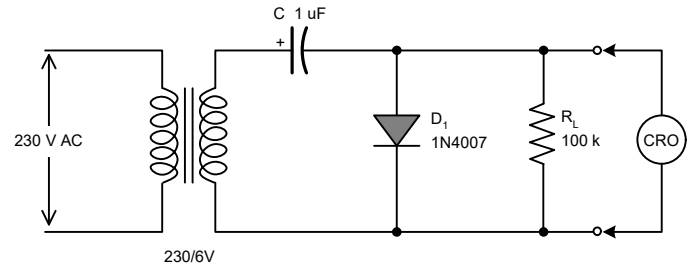


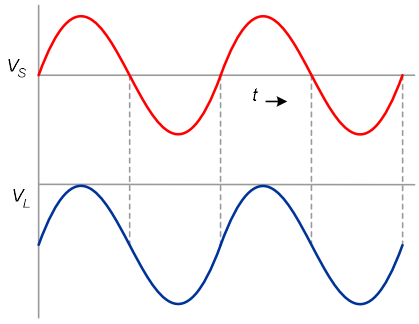
Positive clamping Circuit





Negative clamping Circuit





Experiment No. 2

ZENER REGULATOR

AIM: To setup and study a zener diode shunt regulator and to plot its line and load regulation characteristics.

COMPONENTS REQUIRED: Zener diode, resistor, rheostat, voltmeter, ammeter, DC source and bread board.

THEORY: A zener diode functions as an ordinary diode when it is forward biased. It is a specially designed device to operate in the reverse bias. When it is in the reverse breakdown region, the zener voltage V_z remains almost constant irrespective of the current I_z through it. A series resistor R_s is used to limit the zener current below its maximum current rating. The current through R_s is given by the expression $I_s = I_z + I_L$, where I_L is the current through the load resistor R_L. The value of R_S must be properly selected to fulfil the following condition requirements.

When the input voltage, V_I increases I_L remains the same, I_S and I_Z increases. Similarly if input voltage decreases, I_L remains the same, I_S and I_Z decreases. But if I_Z falls lower than the minimum zener current enough to keep the zener in the breakdown region, the regulation will cease and output voltage decreases. A low input voltage can cause the regulator fail to regulate. The series resistance should be selected between R_{Smax} and R_{Smin} which are given by the expressions,

$$R_{Smin} = [V_{Imax} - V_Z]/I_{Zmax}$$

$$R_{Smax} = [V_{Imin} - V_Z]/[I_{Zmin} + I_L]$$

PROCEDURE:

1. Wire up the circuit on the bread board after testing all the components.
2. Keep the load constant. Note down the output voltage varying input from 8V to 14V in steps of 1V. Plot the line regulation graph with V_i along x-axis and V_o along y-axis. Calculate percentage line regulation using the expression $(\Delta V_o/\Delta V_i)$x100%.
3. 3. Keep the input voltage constant (say 10V) and note down the output voltage for various values of load current starting from 0 to 5 mA, by varying R_L using a rheostat. Plot the load regulation graph with I_L along x-axis and V_o along y-axis.
4. To calculate percentage load regulation, mark V_{NL} and V_{FL} on y-axis on the load regulation graph. V_{NL} is the output voltage in the absence of load resistor and V_{FL} is the output voltage corresponding to rated I_L (here, 5mA). Calculate the percentage load regulation V_R as per the equation,

$$V_R = \frac{V_{NL} - V_{FL}}{V_{NL}} x100\%$$

DESIGN

Assume $V_o = 5.6\,V$, $I_{Lmax} = 5mA$ Input voltage is in the range 8-14V.

Select 5.6V zener [$P_o = 400mW$, $V_Z = 5.6V$, $r_d = 8\Omega$ at $I_Z = 10mA$].

Use 2.4 k rheostat as load resistance load current can be varied from 2.4 mA and upwards.

$$I_{Zmax} = \frac{P_{max}}{V_Z} = \frac{0.4}{5.6} = 71.42mA$$

$$I_{Zmin} = 10\%\ of\ I_{Zmax} = 0.1\ x\ 71.42 = 7.142mA$$

$$R_{Smax} > R_S > R_{Smin}$$

$$R_{Smax} = [V_{Imin} - V_Z]/[I_{Zmin} + I_{Lmax}] = \frac{(8 - 5.6)V}{(7.142 + 5)mA} = 197.6\Omega$$

$$R_{Smin} = [V_{Imax} - V_Z]/I_{Zmax} = \frac{(14 - 5.6)V}{71.42mA} = 117.6\Omega$$

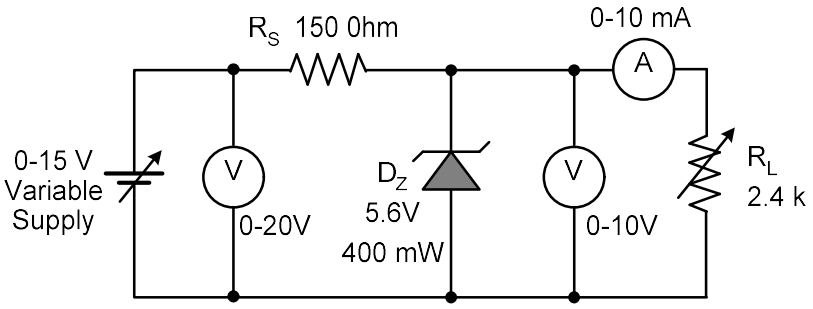
Select $R_S = 150\Omega$

Power rating of R_S

Max current through $R_S = I_m = [V_{Imin} - V_Z]/R_S = \frac{(14-5.6)V}{150\Omega} = 56mA$

Power rating of $R_S = {I_m}^2\ x\ R_S = 0.4704W$ >> Select 150 ohms 0.5W resistor

CIRCUIT DIAGRAM



TABULAR COLOUMNS

LINE REGULATION

Keeping load current constant at $I_L = 5mA$, The input voltage is varied from 8 V to 14V and corresponding observations are made.

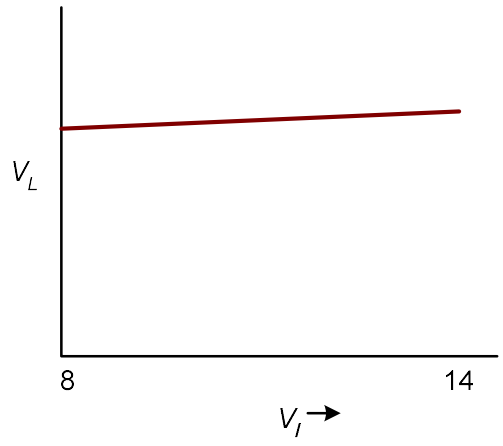
V_{in}(volts)	V_o (volts)

LOAD REGULATION

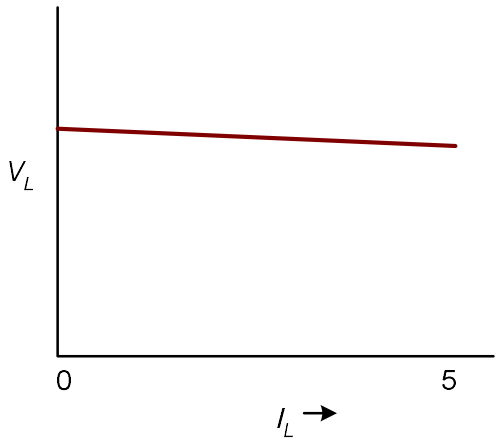
Keeping input voltage at 10V, the load current is varied from 0 to 5 mA and observations are made. For taking reading corresponding to no load ($I_L = 0$), the loading rheostat may be disconnected.

I_L mA	V_o(volts)

EXPECTED OUTPUT PLOTS



Line Regulation



Load Regulation

Experiment No. 3

COMMON EMITTER AMPLIFIER

AIM

1. To design a small signal voltage amplifier.
2. To plot its frequency response and to obtain bandwidth.

THEORY

Amplifiers are classified as small signal amplifiers and large signal amplifiers depending on the shift in operating point, from the quiescent condition caused by the input signal. If the shift is small, amplifiers are referred to as small signal amplifiers and if the shift is large, they are known as large signal amplifiers. In small signal amplifiers, voltage swing and current swing are small. Large signal amplifiers have large voltage swing and current swing and the signal power handled by such amplifiers remain large.

Voltage amplifiers come under small signal amplifiers. Power amplifiers are one in which the output power of the signal is increased. They are called large signal amplifiers. Figure shows the circuit diagram of a common emitter amplifier.

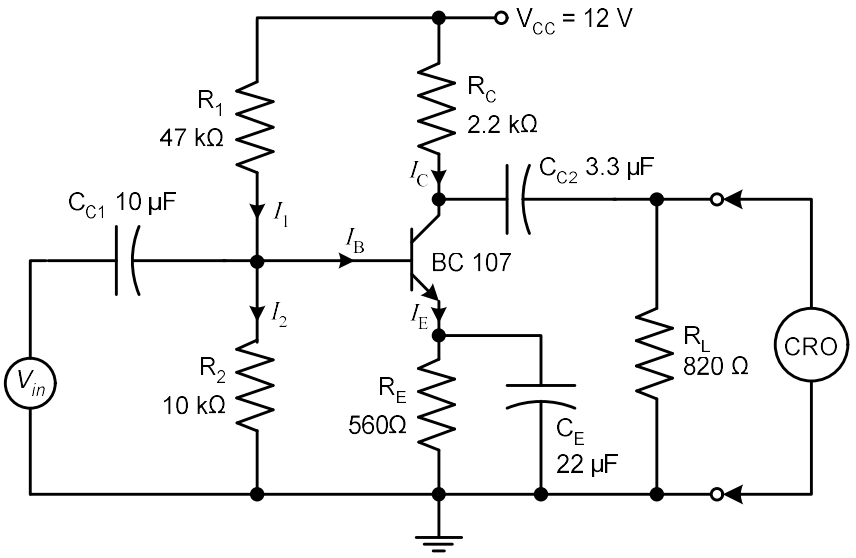


Fig 1. Circuit diagram

DESIGN

From the transistor data sheet, for BC107,

$h_{fe} = \beta = 110$, $I_{c\,max} = 100$ mA, $V_{CE\,max} = 45$V

Let V_{CC} =12V, I_c = 2mA. Since the quiescent point is in the middle of the load line for the amplifier, V_{CE} = 50% of V_{CC} = 6V.

V_{RE} = 10% of V_{CC} = 1.2V.

Assuming $I_C = I_E$, $V_{RE} = I_C R_E = I_E R_E$

$$1.2 = 2 \times 10^{-3} \times R_E$$

$R_E = \frac{1.2}{2\times10^{-3}} = 600\ \Omega$ Select standard value of resistance 560 Ω.

Voltage across collector resistance, $V_{RC} = V_{CC} - V_{CE} - V_{RE}$

$$= 12 - 6 - 1.2 = 4.8 \text{ V}$$

$R_C = \frac{V_{RC}}{I_C} = \frac{4.8}{2\times10^{-3}} = 2.4$ kΩ Select standard value of 2.2 kΩ

$$\text{Base current, } I_B = \frac{I_C}{\beta} = \frac{2 \times 10^{-3}}{110} = 18.2\ \mu\text{A}$$

Take $I_2 = 10I_B$ then $I_1 = 10I_B + I_B = 11I_B$

Base voltage, $V_B = V_{RE} + V_{BE} = 1.2 + 0.6 = 1.8\ V$

$R_2 = \frac{V_B}{I_2} = \frac{1.8}{10\times18.2\times10^{-6}} = 9.9\ k\Omega$ Select standard value of 10 kΩ

$R_1 = \frac{V_{CC}-V_B}{I_1} = \frac{12-\ .8}{11\times18.2\times10^{-6}} = 51\ k\Omega$ Select standard value of 47 kΩ

Design of R_L:

Gain of the common emitter amplifier is given by the expression $A_V = -\left(\frac{r_c}{r_e}\right)$

where $r_c = R_C \parallel R_L$ and $r_e = \frac{25 \text{ mV}}{2 \text{ mA}} = 12.5\ \Omega$

For a gain of 50, substituting it in the expression we get, R_L=873 Ω.

Select standard value of 820 Ω for R_L

Design of coupling capacitors C_{C1} and C_{C2}

X_{C1} should be less than the input impedance of the transistor. Here, R_{in} is the series impedance.

Then $X_{C1} \leq \frac{R_{in}}{10}$

Here $R_{in} = R_1 \parallel R_2 \parallel h_{fe}\ r_e = 47\text{kΩ} \parallel 10\ \text{kΩ} \parallel\ 110 \times 12.5\ \Omega = 1.17$ kΩ

We get R_{in}=1.17 kΩ. Then $X_{C1} \leq 117$ Ω.

For a lower cut off frequency of 200 Hz, $C_{C1} = \frac{1}{2\pi f X_{C1}} = \frac{1}{2\pi\times200\times117} = 6.8$ μF

Select standard value of 10 μF for C_{C1}

Similarly, $X_{C2} \leq \frac{R_{out}}{10}$ where R_{out}=R_C. Then $X_{CE} \leq 220\Omega$.

So, $C_{C2} = \frac{1}{2\pi f\ _{C2}} = \frac{1}{2\pi\times200\times220} = 3.6$ μF

Select standard value of 3.3 μF for C_{C2}

Design of bypass capacitors C_E

To bypass the lowest frequency (say 200 Hz), X_{CE} should be much less than or equal to the resistance R_E.

$$X_{CE} \leq \frac{R_E}{10}$$

$X_{CE} \leq \frac{560}{10}$ ie. $X_{CE} \leq 56$

Apply value of f such that the amplifier has good gain at a lower cutoff frequency of 200 Hz

$$C_E \geq \frac{1}{2\pi f X_{CE}} = \frac{1}{2\pi \times 200 \times 56} = 14.2\ \mu F$$

Select standard value of 22 μF for C_E

FREQUENCY RESPONSE

The gain of an ideal amplifier should remain the same for any frequency of the input signal. Therefore, the frequency response curve (gain in db plotted against frequency) becomes a straight line parallel to the frequency axis.

In actual practice, the coupling capacitors and the emitter bypass capacitor reduce the gain at lower frequencies. The capacitance internal to the transistor and stray capacitance due to the wiring reduce the gain at higher frequencies.

Fig 2 shows the typical frequency response characteristics of CE amplifier. The curve is flat only for middle range of frequencies. There is one low frequency f_L and one high frequency f_H beyond

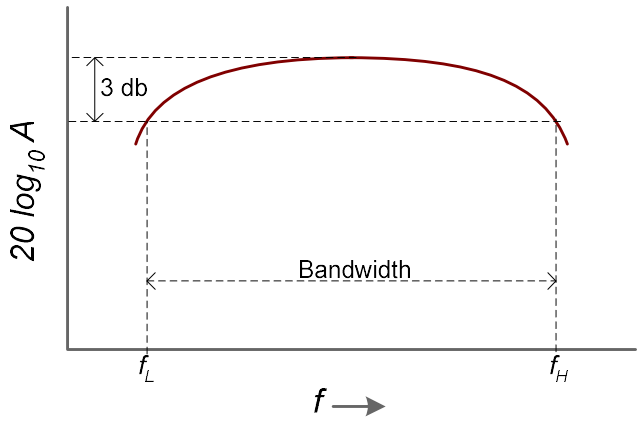


Fig 2. Frequency response

which the gains, A_L and A_H are $1/\sqrt{2}$ times the gain A_M (maximum gain) at the middle frequencies. The two frequencies are called lower and higher cut off frequencies. The difference between them is called the bandwidth.

PROCEDURE

The circuit is set up as shown in figure 1. Input signal V_s is given to the circuit through a signal generator (sinusoidal signal is applied). Measure the magnitude (peak to peak) of the input by using CRO. Connect the CRO to the output side and the amplified output is observed. Increase the frequency in steps and observe the magnitude of V_O. The frequency response is plotted in a semi log sheet.

OBSERVATIONS

Readings are to be taken till Vo decreases appreciably at high frequencies

V_{in} = …….(p-p)(mV)

Frequency f (Hz)	Vo(p-p) (mV)	$\frac{Vo}{Vin}$	Gain in db $20 \log \frac{Vo}{Vin}$

RESULT

The common emitter amplifier is designed, and its frequency response is plotted.

Voltage gain = V_o/V_{in} =

Lower cutoff frequency =

Upper cutoff frequency =

Bandwidth =

QUESTIONS

1. Define β.
2. Explain in detail procedure for measuring β.
3. Using the values of β, determine the value of α.
4. What are the differences, if any in determining the current gain of NPN and PNP transistors?
5. In the circuit, what should be the effect of reversing the polarity of V_{BB}?
6. What is meant by bias stabilization? Why it is used?
7. What is the phase relationship between the input and output signals of CE amplifier?

Experiment No: 4

INTEGRATOR AND DIFFERENTIATOR USING OP-AMP

AIM

To design and set up an integrator and differentiator circuit using op-amp.

APPARATUS REQUIRED

Power supply, CRO, function generator, bread board, op-amp, capacitor and resistors.

THEORY

INTEGRATOR

Refer to the figure 1. This circuit performs the integration of the input waveform. The output voltage V_o can be expressed as $V_o = -\frac{1}{RC}\int V_i dt + k$ where k is the constant of integration which depends upon the value of V_o at $t = 0$. The peak of the output waveform V_T is given by the expression $V_T = \frac{VT}{4R}$, where T is the time period of the input square wave. Integrators are commonly used in analog computers and wave shaping networks.

DIFFERENTIATOR

If the input resistor of the inverting amplifier is replaced by a capacitor, it forms an inverting differentiator. The output of the circuit is the derivative of the input. Gain of the differentiator increases with increase in frequency, which makes the circuit unstable. This is a drawback of the circuit. The output voltage V_o can be expressed as $V_o = -R_F C_i \frac{dV_i}{dt}$. Differentiator functions as high pass filter. At high frequency it becomes unstable and breaks into oscillations. Input impedance decreases with increase in frequency which makes the circuit very susceptible to high frequency noise. Both stability and high frequency noise problems can be reduced significantly by additional circuit elements.

DESIGN AND CIRCUIT DIAGRAMS

DESIGN OF INTEGRATOR

Let the input frequency be 1 kHz. The frequency at which the integrator gives unity gain output is given by, $f = \frac{1}{2\pi R_1 C}$

Let C = 0.01μF. then R_1 = 15.9 kΩ. Use 15 kΩ std.

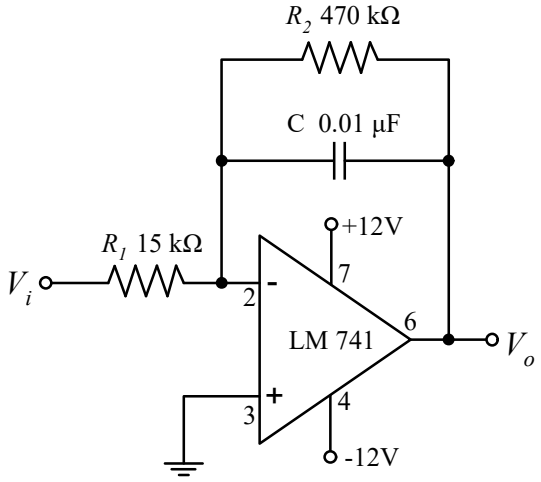


Fig. 1. Circuit diagram of Integrator

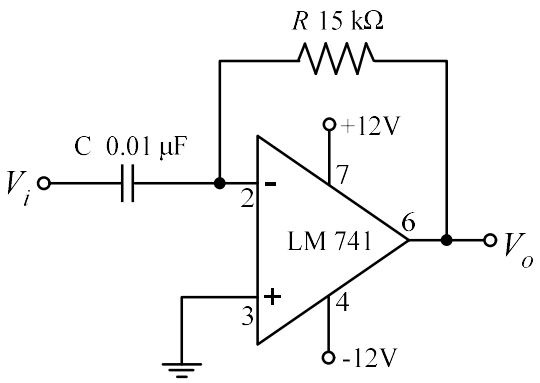


Fig. 2. Circuit diagram of Differentiator

The resistor R_2 in the integrator is provided to attenuate low frequency signals, particularly input dc offset voltage that may be present. Typically, the value of R_2 is selected as 10 times R_1 or more. Select the value of R_2 as 470 k.

DESIGN OF DIFFERENTIATOR

We have, $f = \frac{1}{2\pi RC}$

Let C = 0.01μF. then R = 15.9 kΩ. Use 15 kΩ std.

PROCEDURE

INTEGRATOR

1. Set up the integrator circuit as shown in figure. Give a rectangular wave of ±5V (10V pp) and 1 kHz frequency at the input and observe the input and output simultaneously on CRO.
2. Vary the dc offset of the square wave input and observe the difference in the output waveform.
3. Repeat the experiment by feeding triangular wave and sine wave at the input and observe the output.

DIFFERENTIATOR

1. Set up the differentiator circuit as shown in figure. Give a rectangular wave of ±5V (10V pp) and 1 kHz frequency at the input and observe the input and output simultaneously on CRO.
2. Repeat the experiment by feeding triangular wave and sine wave at the input and observe the output.

WAVEFORMS

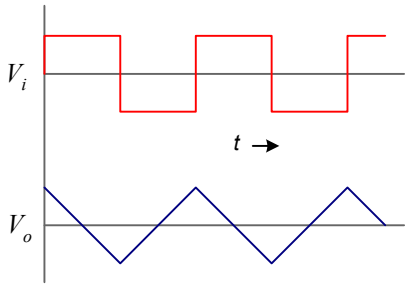


Fig 3. Integrator output

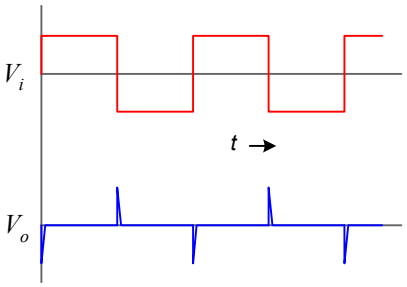


Fig 4. Differentiator output

Experiment No. 5

INVERTING AND NON-INVERTING AMPLIFIER USING OPAMP

AIM

To study the following op-amp circuits

1. Inverting amplifier
2. Non-inverting amplifier

DESIGN

1. Design for inverting amplifier

   The expression for gain is $A_{CL} = -\left(\frac{R_f}{R_1}\right)$

   Let amplifier to be designed with a gain of (-10), select input resistance R_1=10kΩ

   Feedback resistance, $R_f = -(A_{CL} \times R_1)$

   $$= -(-10 \times 10 \times 10^3) = 100\ k\Omega$$

2. Design for non- inverting amplifier

   The expression for gain is $A_{CL} = \left(1 + \frac{R_f}{R_1}\right)$

   Let amplifier to be designed with a gain 11 and select R_1 = 10kΩ

   Feedback resistance, $Rf = (A_{CL} - 1)R_1$

   $$= (10 - 1) \times 10 \times 10^3 = 100\ k\Omega$$

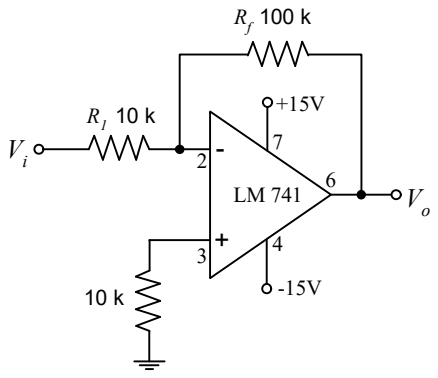


Fig 1. Circuit diagram of inverting amplifier

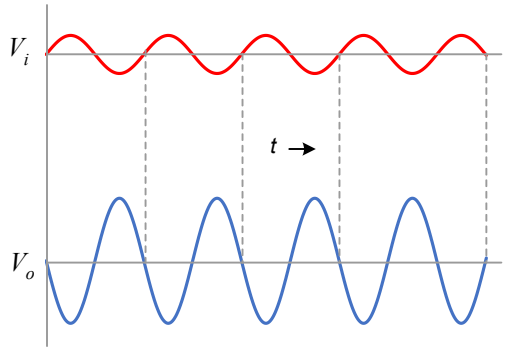


Fig 2. Input and output waveforms of inverting amplifier

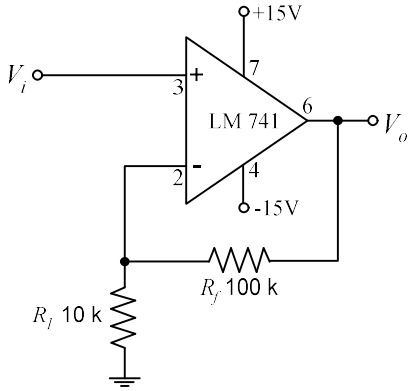


Fig 3. Circuit diagram of non-inverting amplifier

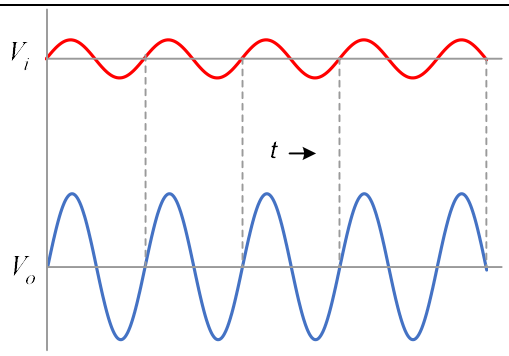


Fig 4. Input and output waveforms of non-inverting amplifier

PROCEDURE

1. Inverting Amplifier

   Set up the circuit as shown in Fig 1. The circuit gives a closed loop gain $A_{CL} = -\left(\frac{R_f}{R_1}\right)$. This gain is very small compared to the open loop gain of the op-amp. Test the circuit by applying the input signal of suitable amplitude (say 1V peak to peak) from a function generator. Observe the output waveform on the CRO and determine actual gain.

2. Non-inverting Amplifier:

   The circuit of a non-inverting amplifier is shown in Fig 3. Its closed loop gain is $A_{CL} = \left(1 + \frac{R_f}{R_1}\right)$. The circuit is tested by applying the input signal of suitable amplitude (say 1V peak to peak) from a function generator. Observe the output waveform on the CRO and determine actual gain.

OBSERVATIONS

Inverting Amplifier

Input Frequency F kHz	Input voltage (p-p) V_i V	Output voltage (p-p) V_o V	Gain $A_{CL} = \frac{V_o}{V_i}$

Non-inverting Amplifier

Input Frequency ***f*** kHz	Input voltage (p-p) $\boldsymbol{V_i}$ V	Output voltage (p-p) $\boldsymbol{V_o}$ V	Gain $A_{CL} = \frac{V_o}{V_i}$

RESULT

The basic op-amp circuits of inverting & non-inverting amplifiers were designed set up and output waveforms were obtained in a CRO. The gain obtained are

Inverting amplifier:

Gain = …….

Non-inverting amplifier:

Gain = …….

Experiment No. 6

SERIES VOLTAGE REGULATOR

AIM

To design and set up a transistor series regulator and plot

1. Load current vs output voltage
2. Input voltage vs output voltage for a constant load current

THEORY

An ideal power supply maintains a constant voltage at its output terminals, no matter what current is drawn from it. The output voltage of a practical power supply changes with load current, generally dropping as load current increases. The power supply specifications include a full load current rating, which is the maximum current that can be drawn from the supply. The terminal voltage when full load current is drawn is called the full load voltage (V_{FL}). The no load voltage (V_{NL}) is the terminal voltage when zero current is drawn from the supply, that is, the open circuit terminal voltage.

One measure of power supply performance, in terms of how well the power supply is able to maintain a constant voltage between no load and full load conditions, is called its percentage voltage regulation.

An unregulated power supply has poor regulation, ie. output voltage changes with load variations. If a power supply has poor regulation it possesses high internal impedance. A simple emitter follower regulator is shown in Fig. 4.1. It is also called a series regulator since the control element (transistor) is in series with the load. It is also called as the pass transistor because it conducts or passes all the load current through the regulator. It is usually a power transistor. The zener diode provides the voltage reference, and the base to emitter voltage of the transistor is the control voltage.

The value of R_S must be sufficiently small, to keep the zener in its reverse breakdown region. Writing Kirchoff's voltage law to the output circuit,

$$V_o + V_{BE} - V_Z = 0$$
$$ie \quad V_{BE} = V_Z - V_o$$

If V_Z is perfectly constant, the above equation is valid at all times, and any change in V_o must cause change in V_{BE}, in order to maintain equality.

When current demand is increased by decreasing R_L, V_o tends to decrease. From the above equation, it is seen that as V_Z is fixed, decrease in V_o increases in V_{BE}. This will increase the forward bias of the transistor, thereby increasing level of conduction. Thus, the output current is increased to keep $I_L R_L$ a constant. The reverse process occurs when R_L is increased. Thus, the above circuit keeps the output voltage constant, even if the load varies widely.

DESIGN

Specifications

Output Voltage, V_o = 5 volts (regulated)

Output Current, I_L = 0 - 30 mA

Input Voltage, V_i = 10-15 V

Maximum power dissipated in the transistor = $(V_{imax} - V_o)\ \underline{I_{max}}$

Select a transistor whose P_{dmax} is greater than the power dissipation calculated above and whose V_{CEO} is greater than $(V_{imax} - V_o)$.

Calculate base current $I_B = I_{max} / h_{FE.min.}$

Select a zener having breakdown voltage equal to

$V_Z = (V_o + 0.6)$ volts

$V_Z = 5 + 0.6 = 5.6$ V

Referring datasheet for zener diodes, power dissipation of the zener diode is found.

The wattage rating of the zener = $V_Z I_{Zmax}$

Select zener diode of 5.6 V, 400mW

Input = 10 – 15 V Output = 0 - 30 mA at 5V

I_B = 30mA / 50 = 0.6 mA

I_{Zmax} = 400 mW / 5.6 V = 71.4 mA

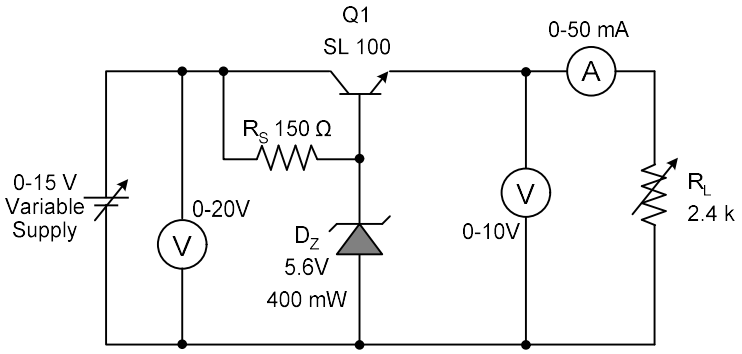


Fig. 1 Circuit diagram of series regulator

I_{Zmin} = 10% of I_{Zmax} = 7.14 mA

$$R_{max} = \frac{V_{i\,min} - V_z}{I_{z\,min} + I_B} = \frac{10 - 5.6}{(7.14 - 0.6) \times 10^{-3}} = 673\ \Omega$$

$$R_{min} = \frac{V_{i\,max} - V_z}{I_{z\,max}} = \frac{15-5.6}{71.4\times10^{-3}} = 132\ \Omega$$

Select R = average of R_{min} and R_{max} = 330 Ω

Power rating of R is to be fixed considering maximum I^2R loss.

Power loss, $I^2R = \left(\frac{V_{i\,max} - V_z}{R}\right)^2 \times R = \frac{15-5.6}{330} = 0.27\ W$

Select R as 330 Ω, 0.5 W

PROCEDURE

Load regulation

1. The circuit is wired as per the circuit diagram shown in fig. 1.
2. Keep the input voltage constant at V_{imin}, ie 10 V.
3. Vary the load resistance. Note I_L and V_O for each setting of R_L. Ensure that V_i remains same throughout.
4. Draw a plot between I_L and V_O.

Line Regulation

Percent line regulation is another measure of the ability of a power supply to maintain a constant output voltage. In this case, it is a measure of how sensitive the output is to the changes in input or line voltage rather than to the changes in load. The specification is usually expressed as the percent change in output voltage that occurs per volt change in input voltage, with the load R_L assumed constant.

1. The circuit diagram is wired as per the circuit diagram shown in fig. 1.
2. Keep the load resistance R_L a constant.
3. Vary the input voltage between the limits for which the regulator is designed (10 to 15V).
4. Note the load voltage V_O for each setting of V_{in}.
5. Draw a graph between V_{in} (X axis) and V_L (Y axis).

OBSERVATIONS

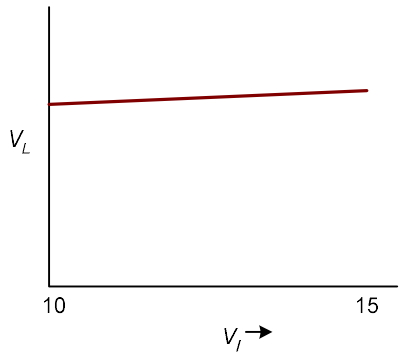
Load Regulation

Load Current I_L mA	Output voltage V_O V

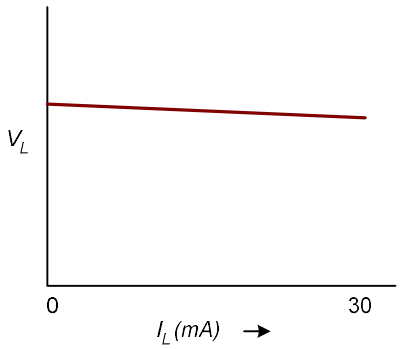
Line Regulation

Input Voltage V_i V	Output voltage V_O V

EXPECTED OUTPUT PLOTS



Line Regulation



Load Regulation

RESULT

Line regulation and load regulation curves are plotted.

QUESTIONS

1. Define percentage line and load regulation, what are the typical values?
2. What are the demerits of a series voltage regulator? How can they be avoided?
3. What is an SMPS? Where is it used?

Experiment No: 7

PRECISION RECTIFIER USING OP-AMP

AIM:

To design and set up precision rectifier using op-amp and check its performance.

EQUIPMENT AND COMPONENTS REQUIRED

Dual power supply, CRO, function generator, bread board, op-amp, diodes, and resistors.

THEORY

In a normal diode rectifier, the cut in voltage across the diode will result in reduction of output voltage and inaccuracy of rectification. If ideal rectifier is needed in an application, a precision rectifier as shown Fig. 1 may be used.

In the circuit, when the input is greater than zero, D1 will conduct and D2 is OFF, so the output is zero because the other end of R2 is connected to the virtual ground and there is no current through R2. When the input is less than zero, D2 is on, and D1 is off, and the output is similar to that of an inverting amplifier with gain $= -\frac{R_2}{R_1}$. The value of R1 and R2 are selected in such a way that the circuit has reasonable level of input impedance and the gain is unity. Diode D1 and D2 are signal diodes.

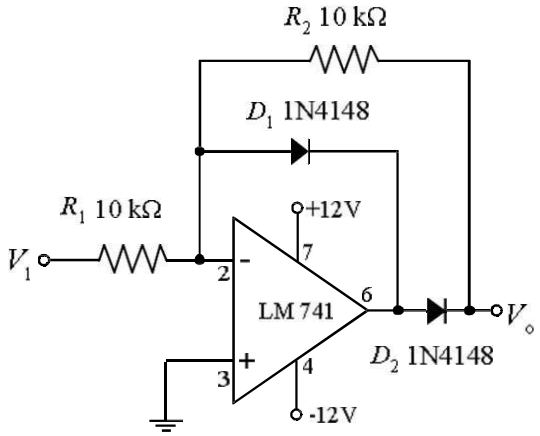


Fig 1. Circuit diagram of Precision Rectifier

PROCEDURE

1. Set up the circuit as shown in figure. Give a sine wave of ±5V peak magnitude and 1 kHz frequency at the input and observe the input and output simultaneously on CRO.

2. Put the CRO into X-Y mode and connect input signal to X and output signal to Y. Select suitable volt per division in both channels and observe the characteristics. The display should look similar to Fig 3.

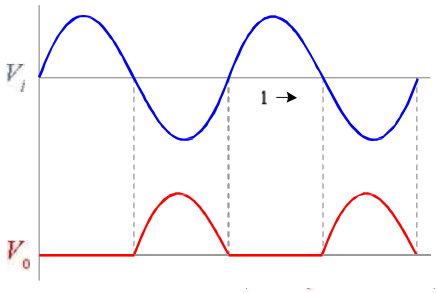


Fig. 2. Input and output waveforms

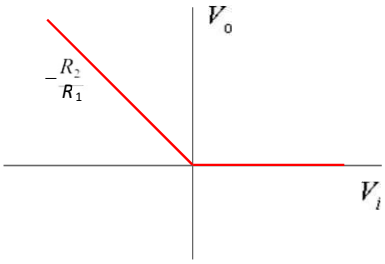


Fig. 3. Transfer characteristics

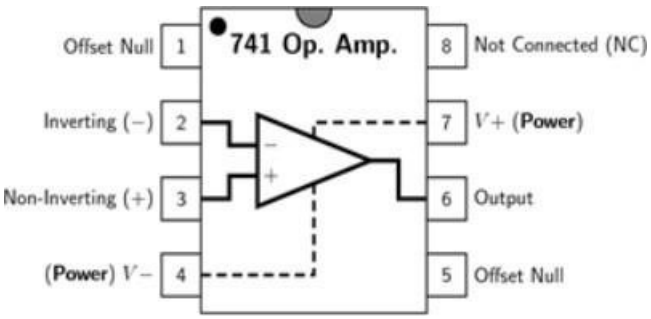


Fig. 4. 741 Op. Amp Pinout Diagram

Experiment No: 8

ASTABLE MULTIVIBRATOR USING IC 555

AIM

To design and set up astable multivibrator of 1000 Hz frequency and 60% duty cycle using IC 555

THEORY

IC 555 timer is an analog IC used for generating accurate time delay or oscillations. The entire circuit is usually housed in an 8-pin package as specified in figures 1 & 2 below. A series connection of three resistors inside the IC sets the reference voltage levels to the two comparators at $\frac{2}{3}V_{CC}$ and $\frac{1}{3}V_{CC}$, the output of these comparators setting or resetting the flip-flop unit. The output of the flip-flop circuit is then brought out through an output buffer stage. In the stable state the $\bar{Q}$ output of the flip-flop is high (ie Q low). This makes the output (pin 3) low because of the buffer which basically is an inverter.The flip-flop circuit also operates a transistor inside the IC, the transistor collector usually being driven low to discharge a timing capacitor connected at pin 7. The description of each pin s described below,

Pin 1: (Ground): Supply ground is connected to this pin.

Pin 2: (Trigger): This pin is used to give the trigger input in monostable multivibrator. When trigger of amplitude greater than (1/3)Vcc is applied to this terminal circuit switches to quasi-stable state.

Pin 3: (Output)

Pin 4 (Reset): This pin is used to reset the output irrespective of input. A logic low at this pin will reset output. For normal operation pin 4 is connected to Vcc.

Pin 5 (Control): Voltage applied to this terminal will control the instant at which the comparator switches, hence the pulse width of the output. When this pin is not used it is bypassed to ground using a 0.01μF capacitor.

Pin 6 (Threshold): If the voltage applied to threshold terminal is greater than (2/3)V_{CC}, upper comparator switches to +Vsat and flip-flop gets reset.

Pin 7: (Discharge): When the output is low, the external capacitor is discharged through this pin

Pin 8 (V_{CC}): The power supply pin

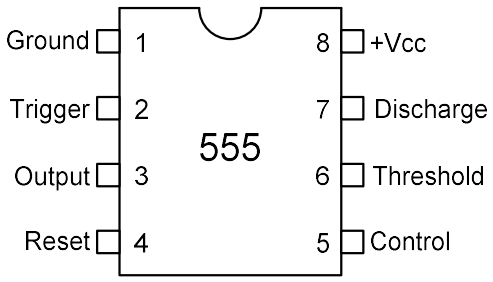


Figure 2: IC 555 pin diagram

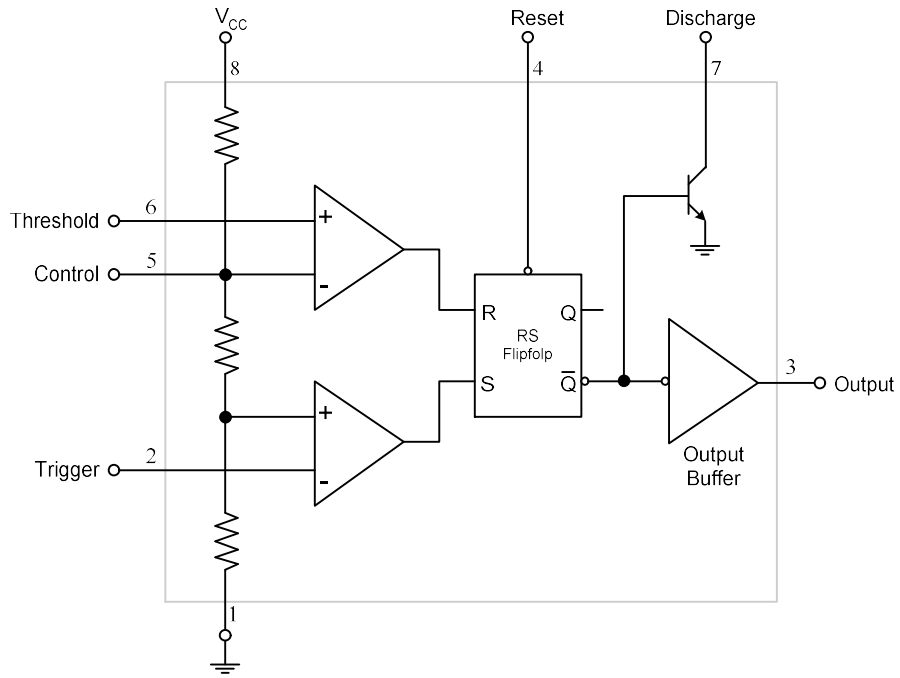


Figure 1: IC 555 Functional block diagram

Astable multivibrator using IC 555

One popular application of the 555 timer IC is as an astable multivibrator or clock Circuit. Figure 3 shows an astable circuit built using 2 external resistors and a capacitor to set the timing interval of the output signal. Capacitor C charges toward V_{CC} through external resistors R_A and R_B. Referring to figure, the capacitor voltage rises until it goes above $\frac{2}{3}V_{CC}$. This voltage is the threshold voltage at pin 6, which drives comparator 1 to trigger the flip-flop(Q low $\bar{Q}$ high) so that the output at pin 3 goes low. In addition, the discharge transistor is driven on, causing the output at pin 7 to discharge the capacitor through resistor R_B. The capacitor voltage then decreases until it drops below the trigger level $\frac{1}{3}V_{CC}$. The flipflop is triggered so that the output goes back high and the discharge transistor is turned off, so that the capacitor can again charge through resistors R_A and R_B towards V_{CC}.

CIRCUIT DIAGRAM & DESIGN

Take $V_{CC} = 10V$ and f = 1000 Hz and duty cycle = 60 %

Then t = 1 ms, t_H = 0.6 ms, t_L = 0.4 ms

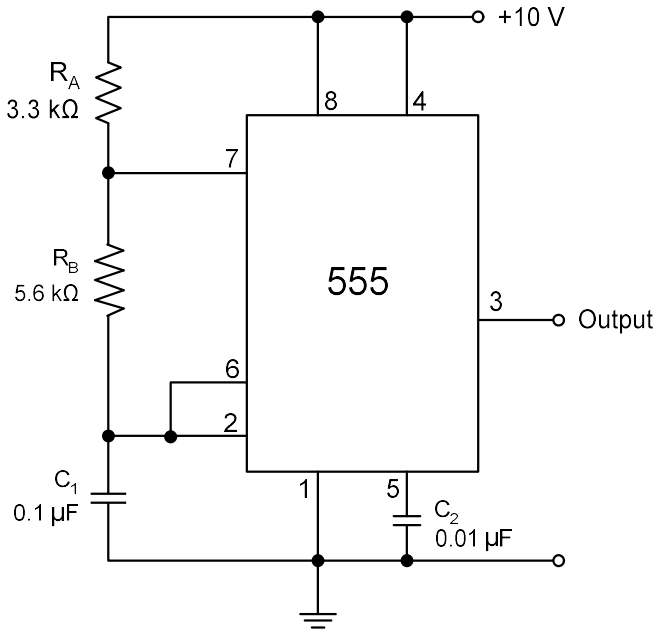


Figure 3 Astable multivibrator circuit using IC 555

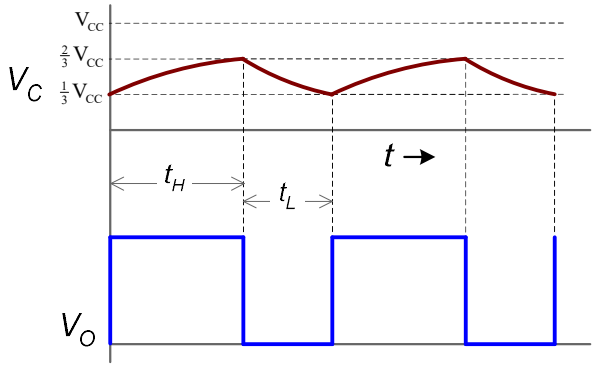


Figure 4 Waveforms of voltage across the capacitor and output voltage

Assume C = 0.1 µF

$t_L = 0.693 \times R_B \times C$ then R_B = 5.77 kΩ take R_B = 5.6 kΩ

$t_H = 0.693 \times (R_A + R_B) \times C$ then R_A = 3.06 kΩ take R_A = 3.3 kΩ

The resistance R_A and R_B should be in the range of 1k to 10k to limit the collector current of the internal transistor.

PROCEDURE

1. Set up the circuit after verifying the condition of IC
2. Observe the waveforms at pin number 3 and 6 of the IC

RESULT

Astable multivibrator using timer IC 555 is designed and setup, and the waveforms are obtained.

Experiment No. 9

PHASE SHIFT OSCILLATOR USING OPAMP

AIM

To design an RC Phase Shift oscillator using op-amp for a given frequency of 1kHz.

THEORY

An oscillator is a circuit that produces a periodic waveform on its output with only the dc supply voltage as a required input. A repetitive input signal is not required but is sometimes used to synchronize oscillations. The output voltage can be either sinusoidal or non-sinusoidal, depending on the type of oscillator. Two major classifications for oscillators are feedback oscillator and relaxation oscillators.

Conditions for oscillation

1. The phase shift around the feedback loop must be effectively zero degrees.
2. The voltage gain, A_{CL} around the feedback loop (loop gain) must equal to (or greater than) one.

The voltage gain around the closed feedback loop, A_{CL}, is the product of the amplifier gain, A_v, and the attenuation, B of the feedback circuit.

$$A_{CL}=A_v B$$

RC phase-shift oscillator is a linear electronic oscillator circuit that produces a sine wave output. It consists of an inverting amplifier element such as a transistor or op-amp with its output fed back to its input through a phase-shift network consisting of resistors and capacitors in a ladder network. Each of the three RC networks in the feedback loop can provide a maximum phase shift approaching 90 degrees. Oscillation occurs at the frequency where the total phase shift through the three RC network is 180 degrees. Inversion output at the output of op-amp itself produces the additional 180 degree to meet the requirement for oscillation of 360 degrees (or zero degree) phase shift around the feedback loop.

DESIGN

The attenuation B of the three section RC feedback network is $B = \frac{1}{29}$

To meet the greater than unity loop gain requirement, the closed loop voltage gain of op-amp must be greater than 29.

Given frequency, f = 1 kHz. We have $f = \frac{1}{2\pi RC\sqrt{6}}$

Let $R_1 = R_2 = R_3 = R$ and $C_1 = C_2 = C_3 = C$

Assume C = 0.01μF.

$$R = \frac{1}{2\pi f\, C\sqrt{6}}$$

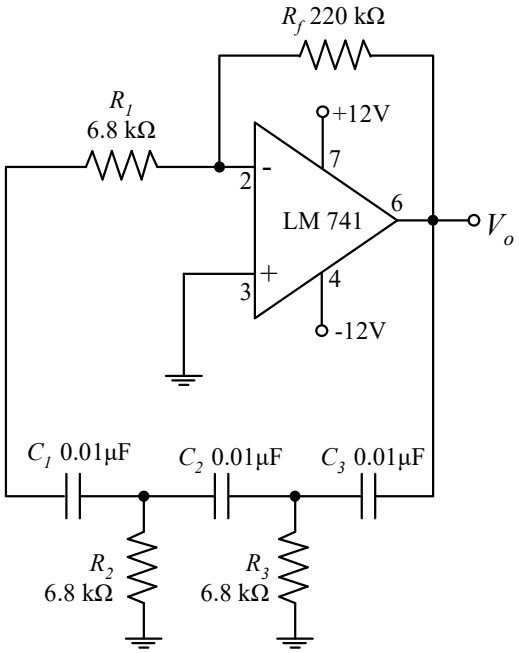
$$= \frac{1}{2\pi \times 10^{3} \times 0.01 \times 10^{-6} \times \sqrt{6}}$$

$$= 6.5\ k\Omega$$

Select nearest value of 6.8 kΩ for R

$$R_f = A_{CL} \times R_1 = 29 \times 6.8 \times 10^{3} = 197.2\ k\Omega$$

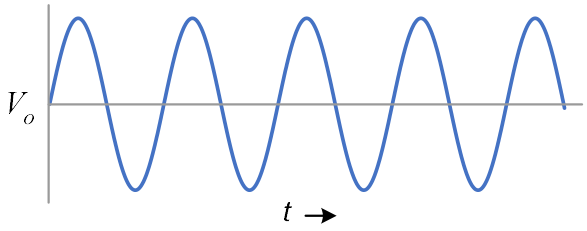
Select nearest value of 220 kΩ for R_f



PROCEDURE:

On a bread board, set up the circuit as shown in the figure. Obtain the sine wave at the output. Check for the frequency obtained.

EXPECTED OUTPUT



RESULT

An RC phase shift oscillator was designed for a frequency of 1kHz.

The observed frequency is _____ kHz

Experiment No. 10

WIEN BRIDGE OSCILLATOR USING OPAMP

AIM:

To design a Wien Bridge oscillator using op-amp for a given frequency of 1kHz.

THEORY:

An oscillator is a circuit that produces periodic electric signals such as sine wave or square wave. The application of oscillator includes sine wave generator, local oscillator for synchronous receivers etc. An oscillator consists of an amplifier and a feedback network.

1. 'Active device' i.e. opamp is used as an amplifier.
2. Passive components such as R-C or L-C combinations are used as feedback network.

To start the oscillation with the constant amplitude, positive feedback is not the only sufficient condition. Oscillator circuit must satisfy the following two conditions known as **Barkhausen** conditions:

1. Magnitude of the loop gain ($A_v \beta$) = 1,

   where, A_v = Amplifier gain and
   β = Feedback gain.
2. Phase shift around the loop must be 360° or 0°.

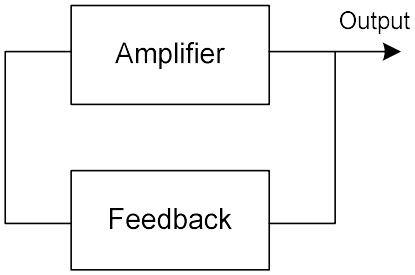


Fig 1. Basic oscillator block diagram

Wien bridge oscillator is an audio frequency sine wave oscillator of high stability and simplicity. The feedback signal in this circuit is connected to the non-inverting input terminal so that the op-amp is working as a non-inverting amplifier. Therefore, the feedback network need not provide any phase shift. The circuit can be viewed as a Wien bridge with a series combination of R_1 and C_1 in one arm and parallel combination of R_2 and C_2 in the adjoining arm. Resistors R_3 and R_4 are connected in the remaining two arms. The condition of zero phase shift around the circuit is achieved by balancing the bridge.

The series and parallel combination of RC network form a lead-lag circuit. At high frequencies, the reactance of capacitor C_1 and C_2 approaches zero. This causes C_1 and C_2 appears short. Here, capacitor C_2 shorts the resistor R_2. Hence, the output voltage V_o will be zero since output is taken across R_2 and C_2 combination. So, at high frequencies, circuit acts as a **'lag circuit'**. At low frequencies, both capacitors act as open because capacitor offers very high reactance. Again, output voltage will be zero because the input signal is dropped across the R_1 and C_1 combination. Here, the circuit acts like a **'lead circuit'**. But at one particular frequency between the two extremes, the output voltage reaches to the maximum value. At this frequency

only, resistance value becomes equal to capacitive reactance and gives maximum output. Hence,

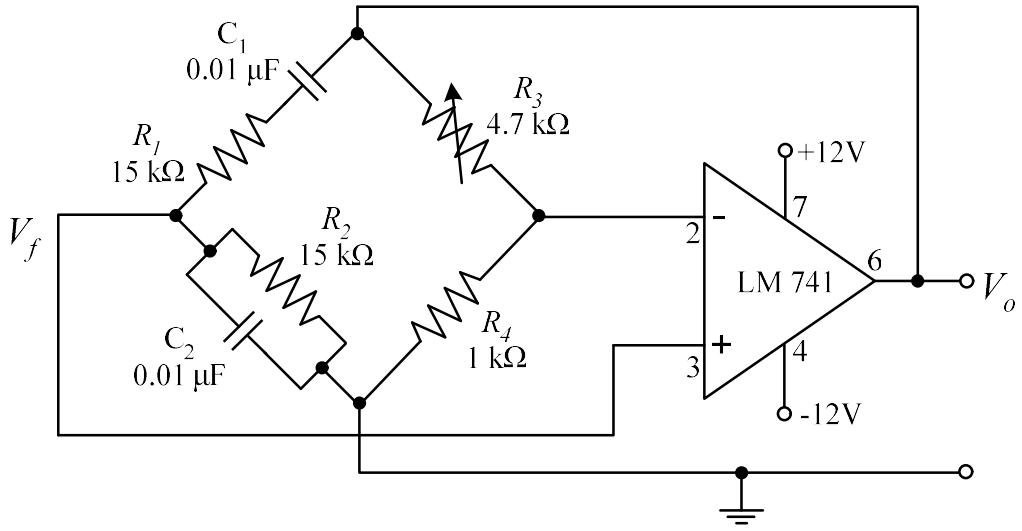


Fig 2 Circuit diagram of Wien bridge oscillator using opamp.

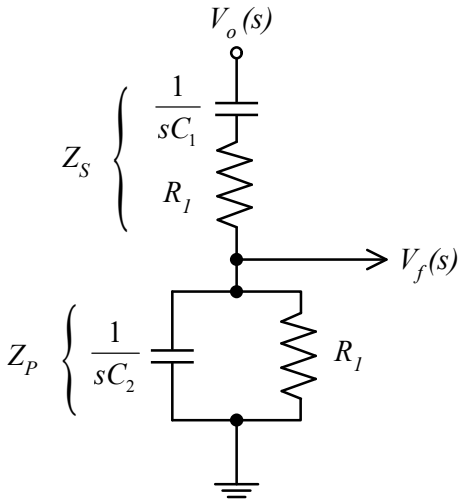


Fig 2 Circuit diagram of Wien bridge oscillator using opamp.

this frequency is known as oscillating frequency (*f*).

Consider the feedback circuit shown in fig 3 On applying voltage divider rule,

$$V_f(s) = \frac{V_o(s) \times Z_P(s)}{Z_P(s) + Z_S(s)}$$

where, $Z_S(s) = R_1 + \frac{1}{sC_1}$ and $Z_P(s) = R_2 \parallel \frac{1}{sC_2}$

Let, $R_1 = R_2 = R$ and $C_1 = C_2 = C$. On solving,

$$\text{feedback gain, } \beta = \frac{V_f(s)}{V_o(s)} = \frac{RsC}{(RsC)^2+3RsC+1} \quad (1)$$

Since the op-amp is operated in the non-inverting configuration the voltage gain,

$$A_v = \frac{V_o(s)}{V_f(s)} = 1 + \frac{R_3}{R_4} \quad (2)$$

Applying the condition for sustained oscillations, $A_v\beta = 1$

Substitute equations (1) & (2), we get,

$$\left(1 + \frac{R_3}{R_4}\right)\left(\frac{RsC}{(RsC)^2 + 3RsC + 1}\right) = 1$$

Substitute $s = j\omega$

$$\left(1 + \frac{R_3}{R_4}\right)\left(\frac{j\omega RC}{-R^2C^2\omega^2 + 3j\omega RC + 1}\right) = 1$$

$$\left(1 + \frac{R_3}{R_4}\right)j\omega RC = (-R^2C^2\omega^2 + 3j\omega RC + 1)$$

$$j\omega\left[\left(1 + \frac{R_3}{R_4}\right)RC - 3RC\right] = 1 - R^2C^2\omega^2$$

To obtain the frequency of oscillation equate the real part to zero.

$$1 - R^2C^2\omega^2 = 0$$
$$\omega = \frac{1}{RC}$$
$$f = \frac{1}{2\pi RC}$$

To obtain the condition for gain at the frequency of oscillation, equate the imaginary part to zero.

$$j\omega\left[\left(1 + \frac{R_3}{R_4}\right)RC - 3RC\right] = 0$$

$$j\omega\left(1 + \frac{R_3}{R_4}\right)RC = j\omega 3RC$$

$$\left(1 + \frac{R_3}{R_4}\right) = 3 \quad (gain\ of\ the\ amplifier)$$

$$\frac{R_3}{R_4} = 2$$

Therefore, $R_3 = 2\,R_4$ is the required condition.

SIMPLIFIED DESIGN:

Frequency of oscillation, $f = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}$

Let, $R_1 = R_2 = R$ and $C_1 = C_2 = C$

$$f = \frac{1}{2\pi RC}$$

Given frequency, f = 1 kHz. assume C = 0.01μF

$$1000 = \frac{1}{2\pi R \times 0.01 \times 10^{-6}}$$

then R = 15.9 kΩ

Take $R_1 = R_2$ = 15 kΩ (nearest standard value)

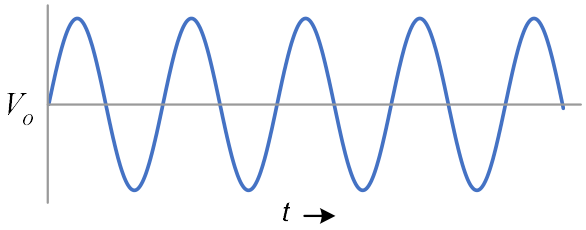
Also, $\frac{R_3}{R_4} = 2$

Let R_4 = 1 kΩ, then R_3 = 2 kΩ. (Use 4.7kΩ potentiometer for fine corrections).

PROCEDURE:

- Test the op-amp by giving a sine wave at the inverting terminal, ground at the non-inverting terminal to obtain a square wave at the output.
- Set up the circuit as shown in the figure.
- Obtain the sine wave at the output. Check for the frequency obtained.

OUTPUT (TO BE OBTAINED):



f = 1 kHz

RESULT:

A Wien bridge oscillator was designed and setup for a frequency of 1kHz and the output waveform is observed.

Experiment No. 11

WAVEFORM GENERATOR USING OPAMP

AIM

To set up and study square waveform, triangular waveform and sawtooth waveform generator using Op-Amp.

THEORY

Square wave oscillator

The basic square wave oscillator is based on the charging and discharging of a capacitor. Op-amps inverting input is the capacitor voltage and the noninverting input is a portion of the output fed back through resistors R_1 and R_2 (refer figure 1). When the circuit is first turned on, the capacitor is uncharged, and thus the inverting input is at 0V. This makes the output a positive maximum, and the capacitor begins to charge towards voltage at V_O through resistor R. When the capacitor voltage reaches a value equal to the feedback voltage (V_f) on the non-inverting input, the op-amp switches to the maximum negative state. At this point, the capacitor begins to discharge from $+V_f$ towards $-V_f$. When the capacitor voltage reaches $-V_f$, the op-amp switches back to the maximum positive state. This action repeats and a square wave output voltage is obtained.

Expression for period is

$T = 2RC\ ln\frac{1+\beta}{1-\beta}$ where $\beta = \frac{R_2}{R_1+R_2}$

If $R_1 = R_2$, the equation for period reduces to $T = 2RC\ ln\,3$

The frequency of oscillation, $f = \frac{1}{2RC\ ln}$

Triangular-wave oscillator

This circuit (figure 2) uses two operational amplifiers. Op-amp A_1 functions as a comparator and the op-amp A_2 as an integrator. Comparator compares the voltage at point P continuously with respect to the voltage at the inverting input; which as at ground potential. When the voltage at P goes slightly below zero, the output of A_1 will switch to negative saturation. Suppose the output of A_1 is at positive saturation $+V_{sat}$. Since this voltage is the input of the integrator, the output of A_2 will be a negative going ramp. Thus, one end of the voltage divider R_1-R_2 is at $+V_{sat}$ and the other at the negative going ramp. At time $t = t_1$, when the negative going ramp attains value of $-V_{ramp}$ the effective voltage at point P becomes slightly less than 0 V. This switches output of A_1 from positive saturation to negative saturation level $-V_{sat}$. During the time when the output of A_1 is at $-V_{sat}$, the output of A_2 increases in positive direction. At the instant $t = t_2$, the voltage at point P becomes just above 0 V, thereby switching the output of A_1 from $-V_{sat}$ to $+V_{sat}$. The cycle repeats and generates a triangular waveform.

At $t = t_1$ $\frac{-V_{ramp}}{R_2} = -\frac{+V_{sat}}{R_1}$ ie. $-V_{ramp} = -\frac{R_2}{R_1}(+V_{sat})$

Similarly, at $t = t_2$ $+V_{ramp} = -\frac{R_2}{R_1}(-V_{sat})$

The peak to peak output of the triangular wave is

$$V_{O(\text{pp})} = +V_{\text{ramp}} - \left(-V_{\text{ramp}}\right) = 2\frac{R_2}{R_1}V_{\text{sat}}$$

During the period *0*-t_1, The integrator functions as below.

$$V_{O(\text{pp})} = \frac{1}{RC}\int_0^{\frac{T}{2}}(-V_{\text{sat}})\ dt = \left(\frac{V_{\text{sat}}}{RC}\right)\left(\frac{T}{2}\right)$$

Then, $T = 2RC\left(\frac{V_{O(\text{pp})}}{V_{\text{sat}}}\right)$

Substituting for $V_{O(\text{pp})}$ $T = \frac{4RCR_2}{R_1}$

Then, frequency of oscillation, $f = \frac{R_1}{4RCR_2}$

Sawtooth-wave oscillator

The difference between the triangular and sawtooth waveform is that the rise time of the triangular wave is always equal to its fall time while in sawtooth wave generator, rise time may be much higher than its fall time or vice versa. The triangular wave generator can be converted to a sawtooth wave generator by injecting a variable dc voltage into the non-inverting terminal of the integrator. This can be done by using a potentiometer as shown in figure 3. When the wiper of the potentiometer is at the centre, the output will be a triangular wave since the duty cycle is 50%. If the wiper moves towards *–V*, the rise time of the sawtooth becomes longer than the fall time. If the wiper moves towards *+V*, the fall time becomes more than the rise time.

DESIGN AND CIRCUIT DIAGRAMS

Design of square wave generator

Let the frequency of oscillation be 1 kHz

Take β = 0.5 and $R_1 = R_2$ = 10 kΩ.

Frequency, $f = \frac{1}{2RC\ ln\,3}$ Assume C = 0.1 μF

Then, $R = \frac{1}{2Cf\ ln} = \frac{1}{2\times0.1\times10^{-6}\times1000\times ln\,3} = 4.55\ \text{k}\Omega$

Select standard value of 4.7 kΩ for *R*.

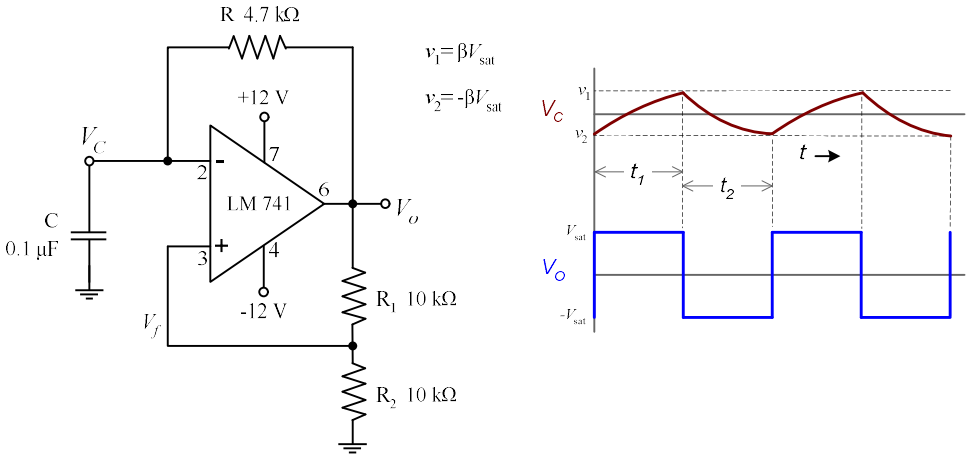


Fig 1. Square wave generator and waveforms

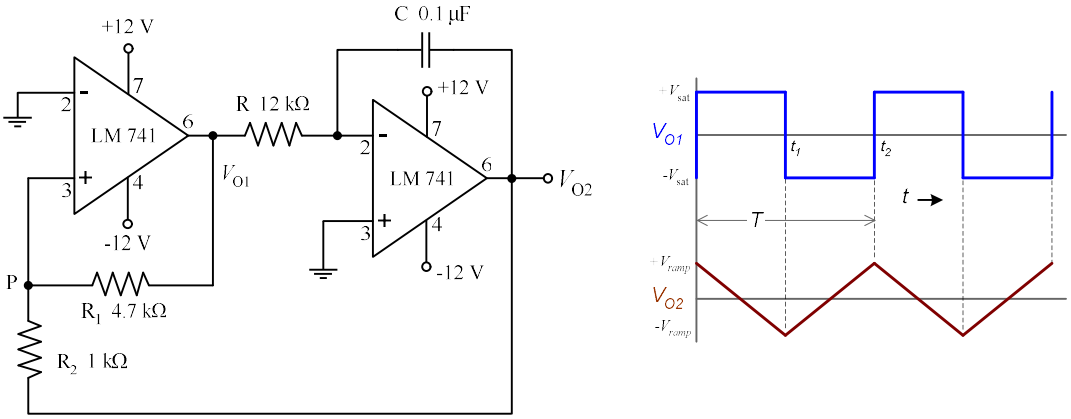


Fig 2. Triangular wave generator and waveforms

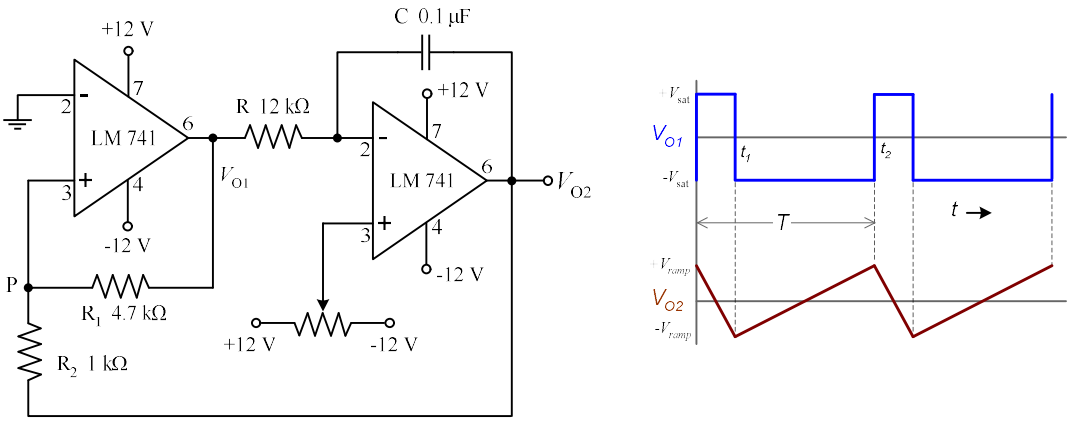


Fig 3. Sawtooth wave generator and waveforms

Design of triangular wave generator

Let the frequency of oscillation be 1 kHz

We have $f = \frac{R_1}{4RCR_2}$ and $V_{O(\text{pp})} = 2\frac{R_2}{R_1}V_{\text{sat}}$

Since supply voltage is ±12 V, V_{sat} will be approximately 10 V

Let $V_{O(\text{pp})}$ be 5 V; Assume R_2 = 1 kΩ.

Then $R_1 = \frac{2V_{\text{sat}}}{V_{O(\text{pp})}}R_2 = \frac{2\times10}{5} \times 1 \times 10^3 = 4$ kΩ

Select standard value, R_1 = 4.7 kΩ

Assume C = 0.1 μF

$$R = \frac{R_1}{4fCR_2} = \frac{4.7\times10^3}{4\times1000\times0.1\times10^{-6}\times1\times10^3} = 11.7 \text{ kΩ}$$

Select standard value, R = 12 kΩ

Design of sawtooth wave generator

Design is similar to that of triangle wave generator.

Select R_3 = 47 kΩ potentiometer to vary the reference voltage of second op-amp.

PROCEDURE

1. Set up the circuit after testing the components.
2. Set up the square wave generator as shown in figure and observe the output waveform and note down their amplitudes and frequencies.
3. Set up the triangular wave generator as shown in figure and observe the variation in frequencies of output waveform by varying the values of resistances R_1, R_2 *and* R_3
4. Set up the sawtooth wave generator as shown in figure and note down the rise time and fall time.
5. Move the wiper of the potentiometer in both directions and observe the changes taking place in the waveform.

RESULT

Circuits of square wave generator, triangular wave generator and sawtooth wave generator are designed, setup and waveforms observed.

Experiment No. 12

COMPARATOR AND SCHMITT TRIGGER CIRCUIT USING OP-AMP

AIM

(i) Study of AC comparator circuit using op amp
(ii) Study of Schmitt trigger using op amp

THEORY

Comparator

A voltage comparator is a two-input circuit that compares the voltage at one input to the voltage at the other input. Usually one input is a reference voltage and the other input a time varying signal. If the time varying input is below or above the reference voltage, then the comparator provides a low or high output accordingly (usually the plus or minus power supply voltages, since the op-amp is used in the open loop configuration, a small difference $(V_+ - V_-)$ makes the output to saturate). For the comparator circuit shown in Figure 1, the output will be at its negative saturation value when the input is greater than the reference and at its positive saturation value when the input is less than the reference. If V_r is zero, the comparator can be used as a zero-crossing detector. If V_r is not zero, the comparator can be referred to as a level detector. One problem encountered with the simple comparator is the instability of its output resulting from noise when the input is in the neighborhood of V_r. The Schmitt trigger provides a method for dealing with this problem.

Schmitt Trigger

Schmitt Trigger circuits are designed with feedback that provides hysteresis in the transfer characteristics. It is basically a comparator with +ve feedback. Figure 4 shows a typical Schmitt trigger circuit along with its transfer characteristic. As the input voltage increases it reaches a threshold voltage (the upper threshold point - UTP) at which the output voltage goes to negative saturation. As the input voltage decreases it reaches another threshold voltage (the lower threshold point - LTP) at which the output voltage goes to positive saturation. With the voltage difference between UTP and LTP larger than the noise, the output remains stable (ie avoids noise triggered oscillation around V_r).

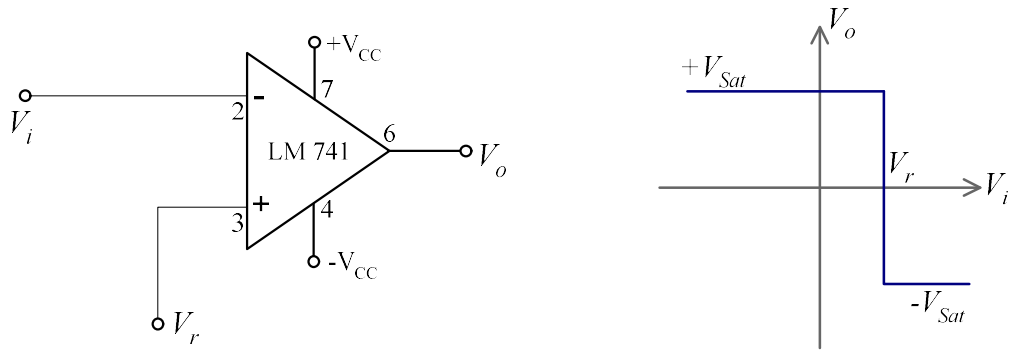


Fig 1: Comparator circuit and transfer characteristics

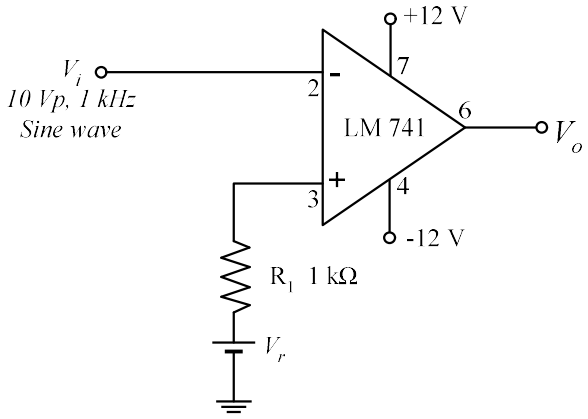


Fig 2. Circuit diagram of comparator

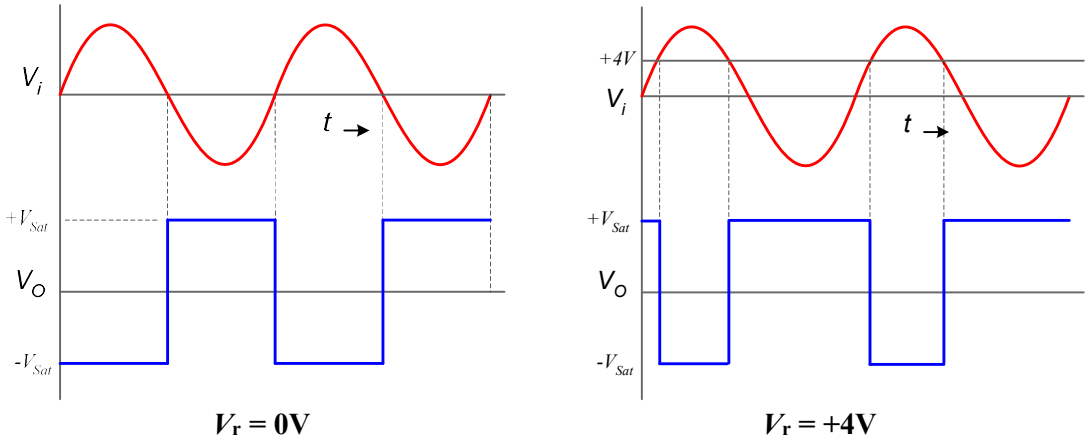


Fig 3. Waveforms comparator

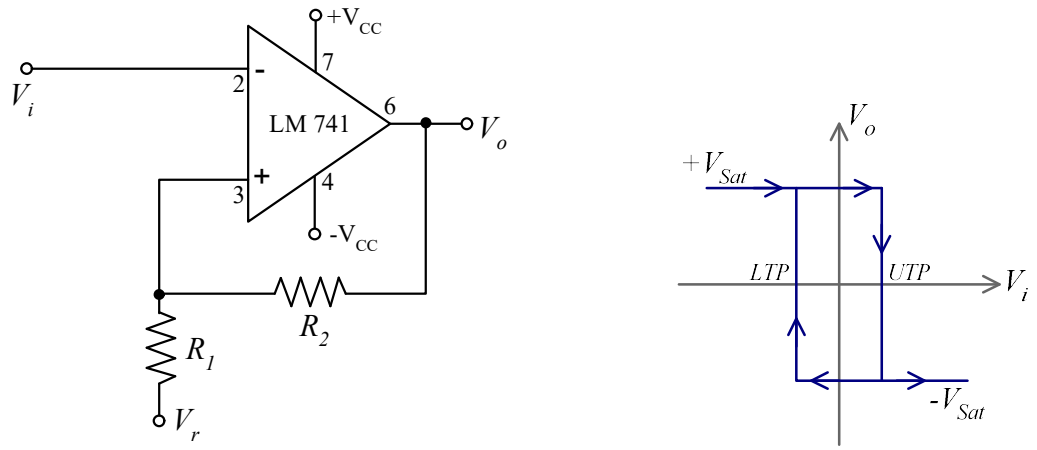


Fig 4: Schmitt trigger and transfer characteristics

SCHMITT TRIGGER DESIGN

Choose LTP = 2V & UTP = 3V. Use a reference voltage source V_r to make polarity of LTP & UTP same (For LTP & UTP with opposite polarity there is no need of V_r).

V_{sat} = 10 V and therefore $V_{out} = \pm 10\ V$

Use superposition theorem to create the following equations:

$$UTP = 3 = \frac{+V_{sat}\ R_1}{R_1 + R_2} + \frac{V_r\ R_2}{R_1 + R_2}$$

$$LTP = 2 = \frac{-V_{sat}\ R_1}{R_1 + R_2} + \frac{V_r\ R_2}{R_1 + R_2}$$

Choose R_2 = 22 kΩ and solve the above equations for R_1 and V_r, we get

R_1= 1.15 kΩ Choose standard value of 1.2 kΩ

V_r = 2.6 V

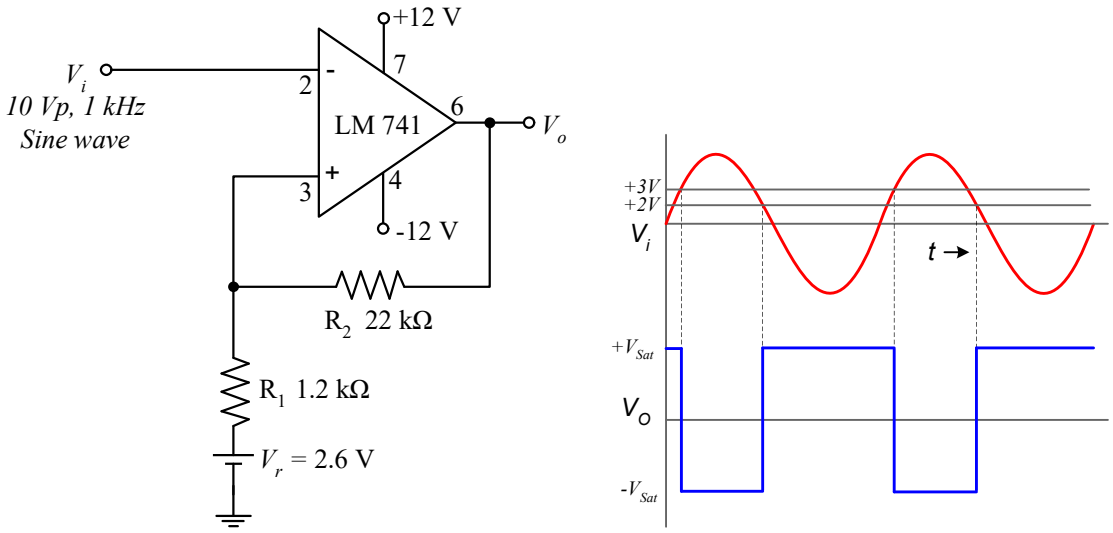


Fig 5. Circuit diagram of Schmitt trigger circuit and waveforms

PROCEDURE

1. Set up circuit as shown in the connection diagram
2. Set the input voltage 20 V peak to peak, 1 kHz in function generator, and apply input signal to the circuit.
3. Observe the output waveform in CRO.
4. Obtain the response for different V_r (for comparator circuit only).

RESULT

AC Comparator and Schmitt trigger circuits were designed and set up. And the output waveform is observed on CRO.

Experiment No. 13

MOSFET AMPLIFIER

AIM:

To obtain the frequency response of MOSFET amplifier in common source configuration with given specifications.

THEORY:

The MOSFET structure has become the most important device structure in the electronics industry. It dominates the integrated circuit technology in Very Large Scale Integrated (VLSI) digital circuits based on n-channel MOSFETs and Complementary n-channel and p-channel MOSFETs (CMOS). The technical importance of the MOSFET results from its low power consumption, simple geometry, and small size, resulting in very high packing densities and compatibility with VLSI manufacturing technology. Two of the most popular configurations of small-signal MOSFET amplifiers are the common source and common drain configurations. The common source circuit is shown below. The common sources, like all MOSFET amplifiers, have the characteristic of high input impedance. High input impedance is desirable to keep the amplifier from loading the signal source. This high input impedance is controlled by the bias resistors R_1 and R_2). Normally the value of the bias resistors is chosen as high as possible. However, too big a value can cause a significant voltage drop due to the gate leakage current. A large voltage drop is undesirable because it can disturb the bias point. For amplifier operation the MOSFET should be biased in the active region of the characteristics.

CIRCUIT DIAGRAM:

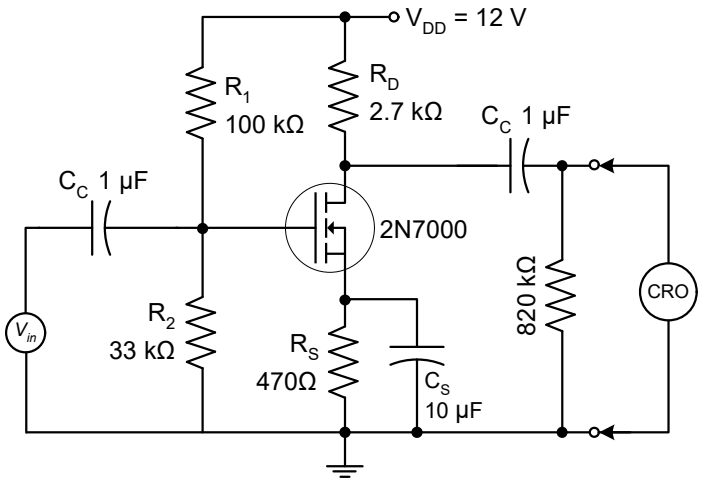


Fig. 1 Circuit diagram of MOSFET amplifier

DESIGN:

Assume V_{DD} = 12V, V_{RD} = 5V, V_{DS} = 6V, I_D = 2 mA

$$R_D = \frac{V_{RD}}{I_D} = \frac{5}{2\times10\times10^{-3}} = 2.5\ \text{k}\Omega$$ use 2.7 kΩ resistor.

Now, the voltage across source side resistance $V_{RS} = V_{DD} - V_{DS} - V_{RD} = 12 - 6 - 5 = 1\ V$

As, $I_S = I_D$, (no current flows through the gate),

$$R_S = \frac{V_{RS}}{I_D} = \frac{1}{2\times10\times10^{-3}} = 500\ \Omega$$ use 470 Ω resistor.

Voltage – divider bias circuit design:

Assume, R_1 = 100 kΩ. By, voltage division rule, R_2 can be obtained as,

$$V_G = V_{DD} \times \frac{R_2}{R_1 + R_2}$$

Selecting the value of V_G as 4V

$$4 = 12 \times \frac{R_2}{100\times10\times10^3 + R_2} \qquad R_2 \approx 47\ \text{k}\Omega$$

Design of capacitors:

Assume impedance of coupling capacitor be < 1.5 kΩ. Therefore,

$X_{C1} \leq 1.5\text{k}\Omega$ ie $\frac{1}{2\pi f C_1} \leq 1.5\ \text{k}\Omega$

Given, the frequency of the input signal is 100Hz.

C_1 = 1.06μf. use 1 μf capacitor.

Let $C_1 = C_2$ = 1 μf.

For the bypass capacitor,

$X_{CS} \leq 150\Omega$ ie $\frac{1}{2\pi f C_S} \leq 150\ \Omega$

C_S = 10μf

PROCEDURE:

Set up the circuit as shown in the figure with an input signal of 0.2V (peak-to-peak) at 1000 Hz. Observe the output on the CRO. Vary the frequency of the input signal over a range of values (from 50Hz to a few MHz) to obtain the frequency response which is a graph between log f (x-axis) and gain in dB (y-axis).

OBSERVATION:

Frequency f Hz	Input voltage V_i V	Output voltage V_i V	Gain $\frac{V_o}{V_i}$ -	Gain $20\,log\,\frac{V_o}{V_i}$ dB

GRAPH (to be obtained):

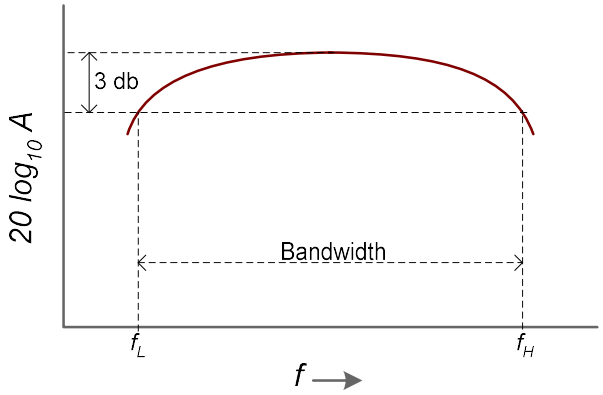


Fig 2. Frequency response

RESULT:

The required common source MOSFET amplifier was designed and set up to obtain the required frequency response.

Experiment No. 14.

BASIC RC CIRCUITS – HIGH PASS AND LOW PASS FILTERS

Aim:

1. To design and set up RC low pass filter for a 3-dB frequency of 1 kHz and study the frequency response.
2. To design and set up RC high pass filter for a 3-dB frequency of 1 kHz and study the frequency response.

Components and equipments required:

Capacitor, resistor, function generator, breadboard and DSO.

Theory:

Filters are the networks designed to pass only certain desired frequency band. It can be broadly classified as passive or active filters according to the devices used to implement them. Filters can also be classified according to the frequency spectrum it passes such as low pass, high pass, band pass and band reject filters.

In RC low pass filter, since the reactance of the capacitor C decreases with increasing frequency, it passes low frequency readily and attenuates high frequencies. At high frequencies the capacitor acts as a virtual short and output falls to zero.

For a sinusoidal input V_{in}, the output signal V_o decreases with increasing frequency. The magnitude of the ratio of output voltage to input voltage of the circuit is given by

$$A = \frac{1}{\sqrt{\left(1 + \frac{f}{f_H}\right)^2}}$$

Where $f_H = \frac{1}{2\pi RC}$ and f is input signal frequency .

At the frequency f_H, the gain falls to 0.707 of its value at low frequency. Hence f_H is called upper 3-dB frequency.

A high pass filter can be made from the low pass filter by merely interchanging its resistance and capacitor. Since the reactance of the capacitor decreases with increase in frequency, the higher frequency components in the input signal appear at the output with less attenuation than the low frequency components. In other words, lower frequencies are attenuated by the circuit. At high frequencies, the capacitor acts as a short circuit and virtually the input amplitude appears at the output.

The magnitude of the ratio of output voltage to input voltage of the circuit is given by

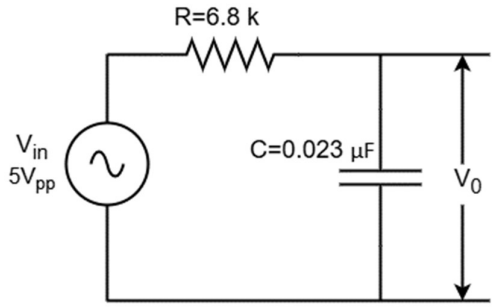
$$A = \frac{1}{\sqrt{\left(1 + \frac{f_L}{f}\right)^2}}$$

Where $f_L = \frac{1}{2\pi RC}$ and f is input signal frequency.

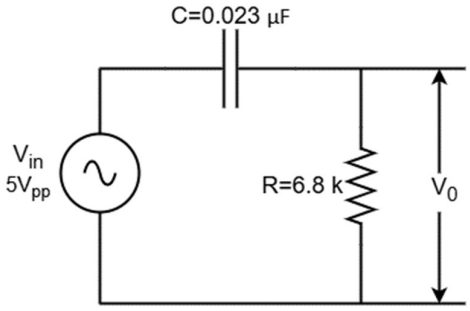
At the frequency f_L, the gain falls to 0.707 of its value at low frequency. Hence f_L is called lower 3-dB frequency.

Circuit Diagram

RC Low pass filter



RC High pass filter



Design

Let the cut off frequency be 1 kHz.

We have $f_L = \frac{1}{2\pi RC}$. and $f_H = \frac{1}{2\pi RC}$

To avoid loading, as a thumb rule, select R = ten times the output impedance of the function generator. i.e. R = 6000 Ω. Use 6.8 k std.

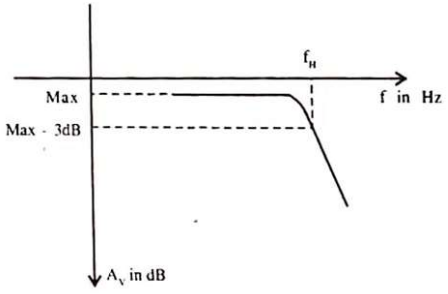
Substituting this in the above expression we get, C = 0.023 µF. Use 0.022 µF.

Procedure

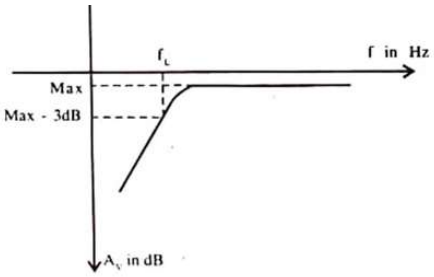
1. Set up the circuit after testing all components and probes.
2. Set the input sine wave voltage at 5 V peak to peak and observe the input and output on the two channels of the DSO.
3. Vary the input frequency from 10 Hz to 100 Hz or more and note down the output voltage in tabular column.
4. Plot the graph on semilog graph sheet with f (or log f) on x-axis and gain in dB on y-axis.
5. Mark a point on graph at 3-dB less than the maximum gain. Extend the point to x-axis

and mark the upper 3-dB frequency.

Sample graph



RC low pass filter



RC high pass filter

Observation

RC Low pass filter

V_{in}=5 V_{pp}

f in Hz	V_o in volts	A_V in dB

RC High pass filter

V_{in}=5 V_{pp}

f in Hz	V_o in volts	A_V in dB

Graph

Result

RC low pass filter

Theoretical 3-dB frequency = ……Hz

Observed 3-dB frequency = ……...Hz

RC high pass filter

Theoretical 3-dB frequency = ……Hz

Observed 3-dB frequency = ……...Hz

Experiment No. 15

Introduction to PCB layout software.

PCB layout software is a specialized tool used to design the physical layout of electronic circuits on a printed circuit board (PCB). It allows engineers to create schematics, place components, route traces (conductive pathways), and generate manufacturing files. This software is crucial for visualizing, designing, and testing circuit board designs before physical prototyping.

Aim: To perform design of PCB

Link to download software and tutorials

https://www.kicad.org/download/windows/

https://www.kicad.org/help/learning-resources/