Experiment No. 4

COMMON EMITTER AMPLIFIER

AIM

1. To design a small signal voltage amplifier.
2. To plot its frequency response and to obtain bandwidth.

THEORY

Amplifiers are classified as small signal amplifiers and large signal amplifiers depending on the shift in operating point, from the quiescent condition caused by the input signal. If the shift is small, amplifiers are referred to as small signal amplifiers and if the shift is large, they are known as large signal amplifiers. In small signal amplifiers, voltage swing and current swing are small. Large signal amplifiers have large voltage swing and current swing and the signal power handled by such amplifiers remain large.

Voltage amplifiers come under small signal amplifiers. Power amplifiers are one in which the output power of the signal is increased. They are called large signal amplifiers. Figure shows the circuit diagram of a common emitter amplifier.

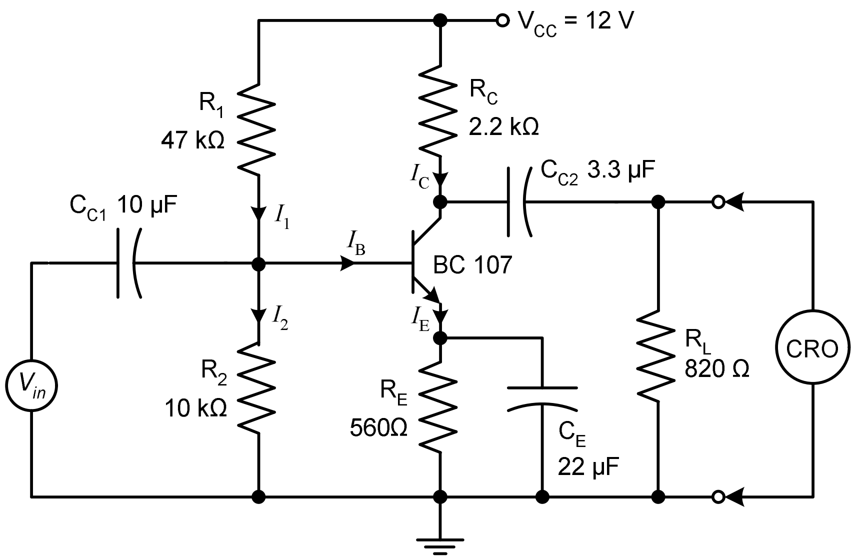

Fig 1. Circuit diagram

DESIGN

From the transistor data sheet, for BC107,

$h_{fe} = \beta = 110$, $I_{c\,max}$=100 mA, $V_{CE\,max} = 45V$

Let V_{CC} =12V, I_c = 2mA. Since the quiescent point is in the middle of the load line for the amplifier, V_{CE} = 50% of V_{CC} = 6V.

V_{RE} = 10% of V_{CC} = 1.2V.

Assuming $I_C = I_E$, $V_{RE} = I_C R_E = I_E R_E$

$1.2 = 2\times10^{-3}\times R_E$

$R_E = \dfrac{1.2}{2\times10^{-3}} = 600\ \Omega$ Select standard value of resistance 560 Ω.

Voltage across collector resistance, $V_{RC} = V_{CC} - V_{CE} - V_{RE}$

$= 12 - 6 - 1.2 = 4.8\ \text{V}$

$R_C = \dfrac{V_{RC}}{I_C} = \dfrac{4.8}{2\times10^{-3}} = 2.4\ \text{k}\Omega$ Select standard value of 2.2 kΩ

Base current, $I_B = \dfrac{I_C}{\beta} = \dfrac{2\times10^{-3}}{110} = 18.2\ \mu\text{A}$

Take $I_2 = 10I_B$ then $I_1 = 10I_B + I_B = 11I_B$

Base voltage, $V_B = V_{RE} + V_{BE} = 1.2 + 0.6 = 1.8\ \text{V}$

$R_2 = \dfrac{V_B}{I_2} = \dfrac{1.8}{10\times18.2\times10^{-6}} = 9.9\ \text{k}\Omega$ Select standard value of 10 kΩ

$R_1 = \dfrac{V_{CC} - V_B}{I_1} = \dfrac{12-1.8}{11\times18.2\times10^{-6}} = 51\ \text{k}\Omega$ Select standard value of 47 kΩ

Design of R_L:

Gain of the common emitter amplifier is given by the expression $A_V = -\left(\dfrac{r_c}{r_e}\right)$

where $r_c = R_C \,||\, R_L$ and $r_e = \dfrac{25\ \text{mV}}{2\ \text{mA}} = 12.5\ \Omega$

For a gain of 50, substituting it in the expression we get, R_L=873 Ω.

Select standard value of 820 Ω for R_L

Design of coupling capacitors C_{C1} and C_{C2}

X_{C1} should be less than the input impedance of the transistor. Here, R_{in} is the series impedance.

Then $X_{C1} \le \dfrac{R_{in}}{10}$

Here $R_{in} = R_1 \,||\, R_2 \,||\, h_{fe}\, r_e = 47\text{k}\Omega \,||\, 10\ \text{k}\Omega \,||\, 110\times12.5\ \Omega = 1.17\ \text{k}\Omega$

We get R_{in}=1.17 kΩ. Then $X_{C1} \le 117\ \Omega$.

For a lower cut off frequency of 200 Hz, $C_{C1} = \dfrac{1}{2\pi f X_{C1}} = \dfrac{1}{2\pi\times200\times117} = 6.8\ \mu\text{F}$

Select standard value of 10 μF for C_{C1}

Similarly, $X_{C2} \le \frac{R_{out}}{10}$ where $R_{out}=R_C$. Then $X_{CE} \le 220\Omega$.

So, $C_{C2} = \frac{1}{2\pi f X_{C2}} = \frac{1}{2\pi \times 200 \times 220} = 3.6\ \mu F$

Select standard value of 3.3 μF for C_{C2}

Design of bypass capacitors C_E

To bypass the lowest frequency (say 200 Hz), X_{CE} should be much less than or equal to the resistance R_E.

$$X_{CE} \le \frac{R_E}{10}$$

$$X_{CE} \le \frac{560}{10} \qquad \text{ie. } X_{CE} \le 56$$

Apply value of f such that the amplifier has good gain at a lower cutoff frequency of 200 Hz

$$C_E \ge \frac{1}{2\pi f X_{CE}} = \frac{1}{2\pi \times 200 \times 56} = 14.2\ \mu F$$

Select standard value of 22 μF for C_E

FREQUENCY RESPONSE

The gain of an ideal amplifier should remain the same for any frequency of the input signal. Therefore, the frequency response curve (gain in db plotted against frequency) becomes a straight line parallel to the frequency axis.

In actual practice, the coupling capacitors and the emitter bypass capacitor reduce the gain at lower frequencies. The capacitance internal to the transistor and stray capacitance due to the wiring reduce the gain at higher frequencies.

Fig 2 shows the typical frequency response characteristics of CE amplifier. The curve is flat only for middle range of frequencies. There is one low frequency f_L and one high frequency f_H

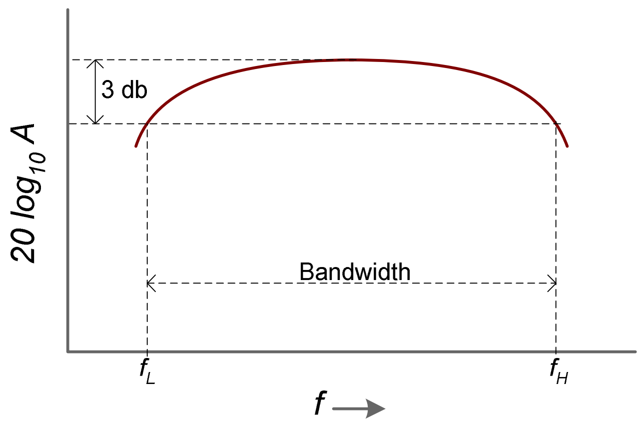

Fig 2. Frequency response

beyond which the gains, A_L and A_H are $1/\sqrt{2}$ times the gain A_M (maximum gain) at the middle frequencies. The two frequencies are called lower and higher cut off frequencies. The difference between them is called the bandwidth.

PROCEDURE

The circuit is set up as shown in figure 1. Input signal V_s is given to the circuit through a signal generator (sinusoidal signal is applied). Measure the magnitude (peak to peak) of the input by using CRO. Connect the CRO to the output side and the amplified output is observed. Increase the frequency in steps and observe the magnitude of V_O. The frequency response is plotted in a semi log sheet.

OBSERVATIONS

Readings are to be taken till Vo decreases appreciably at high frequencies

V_{in} = ……………….(p-p)(mV)

Frequency f (Hz)	Vo(p-p) (mV)	$\frac{Vo}{Vin}$	Gain in db 20 log $\frac{Vo}{Vin}$

RESULT

The common emitter amplifier is designed, and its frequency response is plotted.

Voltage gain = V_o/V_{in} =

Lower cutoff frequency =

Upper cutoff frequency =

Bandwidth =

QUESTIONS

1. Define β.
2. Explain in detail procedure for measuring β.
3. Using the values of β, determine the value of α.
4. What are the differences, if any in determining the current gain of NPN and PNP transistors?
5. In the circuit, what should be the effect of reversing the polarity of V_{BB}?
6. What is meant by bias stabilization? Why it is used?
7. What is the phase relationship between the input and output signals of CE amplifier?