Closed Loop Control of DC Drives

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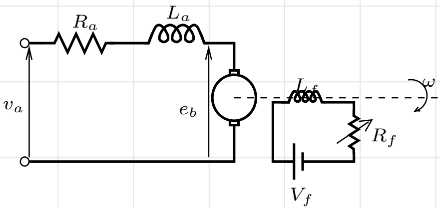
Contents

Separately Excited DC motor



L_a–> Armature Inductance
R_a–> Armature Resistance
e_b–> Back-emf
J–> Moment of Inertia
m_d & m_l–>Developed and Load Torques

Dynamic Equations

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\begin{aligned}
L_a \frac{di_a}{dt} + R_a \cdot i_a + e_b &= v_a \\
e_b &= c_1 \cdot \phi \cdot \omega \\
J \frac{d\omega}{dt} &= m_d - m_l \\
m_d &= c_2 \cdot \phi \cdot i_a \\
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Where, $c_1 = c_2 = c$ for proper SI units.

$$\therefore e_b = c \cdot \phi \cdot \omega, \quad \& \quad m_d = c \cdot \phi \cdot i_a$$

For separately excited dc motor, ϕ is constant.
Hence, $c \cdot \phi = c_\phi$ Where, 'c_ϕ' is the Back-emf constant (V/(rad/s)), as well as the Torque constant (N-m/A).

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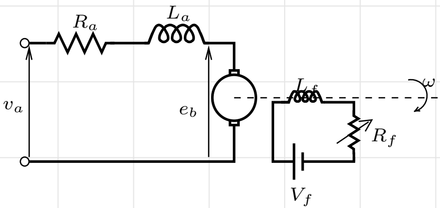

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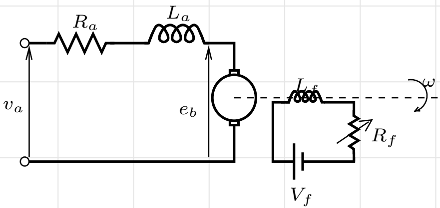

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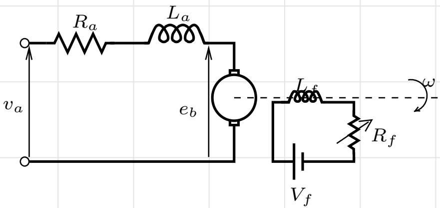

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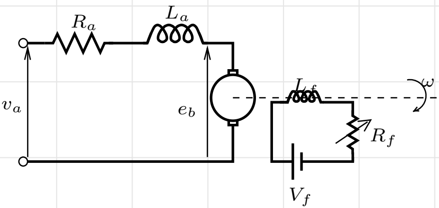

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Transfer Functions of DC motor

- Time-domain block-diagram representation
- s-domain block-diagram representation
- One mechanical Output (ω) and One electrical Output (i_a)
- One mechanical Input (m_l) and One electrical input (v_a)

Transfer Functions

- $F_1\left(s\right) = \frac{\Omega(s)}{V_a(s)}$
- $F_2\left(s\right) = \frac{I_a(s)}{V_a(s)}$
- $F_3\left(s\right) = \frac{\Omega(s)}{M_l(s)}$
- $F_4\left(s\right) = \frac{I_a(s)}{M_l(s)}$

From these transfer functions, the various time-responses as well as steady-state responses can be obtained.
(Final Value Theorem)

$$F_1\left(s\right) = \frac{1/c_\phi}{\left(\frac{JR_a}{{c_\phi}^2}\right)\cdot s\cdot(1+sT_a)+1}$$

$\frac{JR_a}{{c_\phi}^2} = T_{em}$: electro-mechanical time-constant

$$F_2\left(s\right) = \frac{1}{R_a}\cdot\frac{sT_{em}}{sT_{em}(1+sT_a)+1}$$

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The plant dynamics

The Characteristic Equation:

$$s^2 + s\left(\frac{1}{T_a}\right) + \frac{1}{T_a T_{em}}$$

Standard Second-Order Equation:

$$s^2 + 2\zeta\omega_n s + {\omega_n}^2$$

$\Rightarrow$

$$\begin{aligned}\omega_n &= \frac{1}{\sqrt{T_a T_{em}}} \\ \zeta &= \frac{1}{2}\sqrt{\frac{T_{em}}{T_a}}\end{aligned}$$

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In terms of motor-parameters:

$$\begin{aligned} \omega_n &= \frac{c_\phi}{\sqrt{J L_a}} \\ \zeta &= \frac{1}{2}\frac{R_a}{c_\phi}\sqrt{\frac{J}{L_a}} \end{aligned}$$

The plant dynamics

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The roots of the characteristic equation:

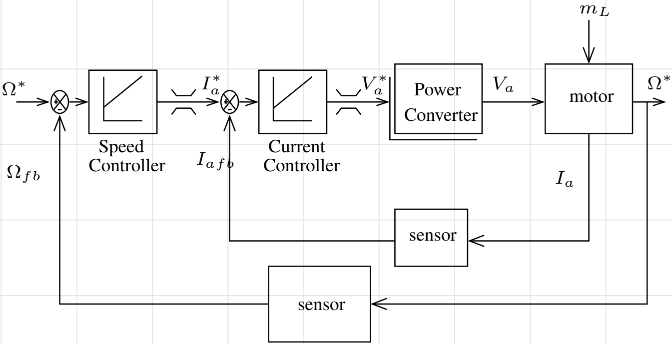
$$s_{1,2} = -\frac{1}{2T_a} \pm \frac{1}{2T_a}\sqrt{1 - \frac{4T_a}{T_{em}}}$$

For $\frac{T_{em}}{T_a} < 4$, the plant (motor) is under-damped.
The motor parameters R_a, L_a, J etc can be obtained from experiments.

Why Cascade Control?

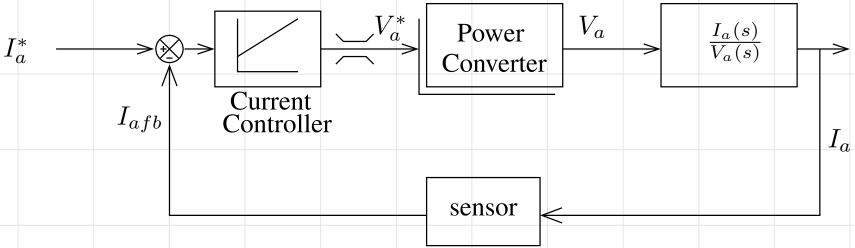
- Requirements of a drive
  - Position control
  - Speed control
  - Acceleration control
  - Torque/current control
  - Overload protection
  - Four quadrant operation
- Cascade control
  - Torque –>Acceleration –>Speed –> Position
  - Bandwidth requirements: High –> Low
  - Design steps: First –> Last
  - Slow response: Use feed-forward in references!

Closed-loop Block diagram



- Two loops
- Design the faster inner-loop first : The current loop
- The relevant transfer function: $F_2(s) = \frac{I_a(s)}{V_a(s)}$

Current-loop Block diagram



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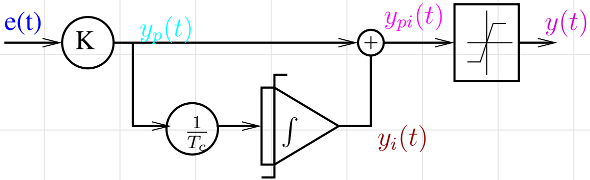
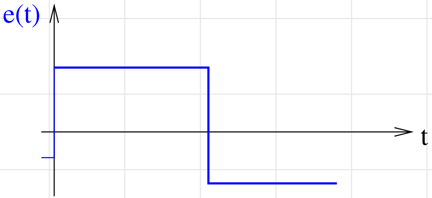
PI Controller

- Zero steady state error
- Better stability prospects compared to I - controller





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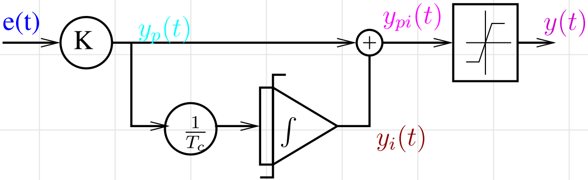

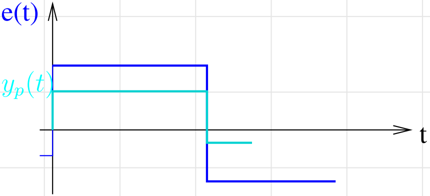

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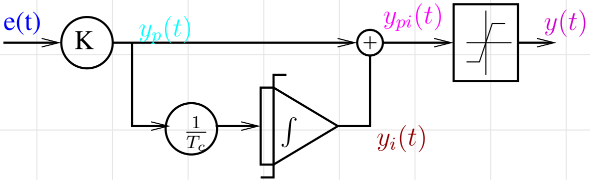

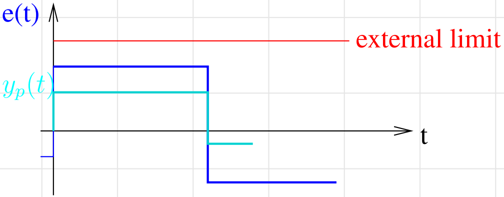

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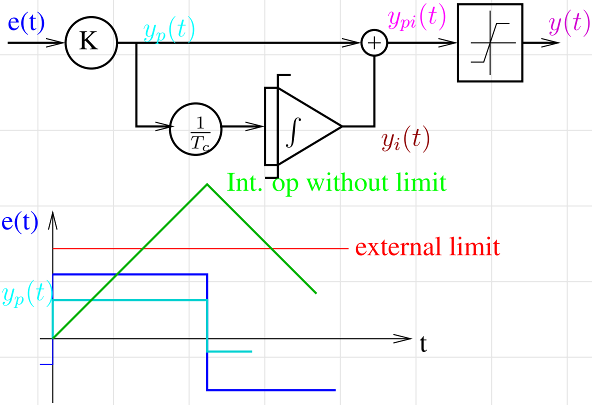

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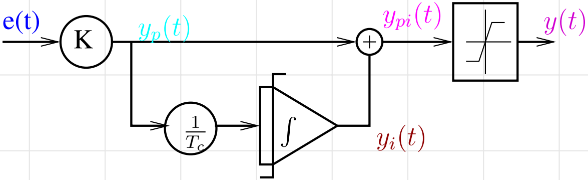

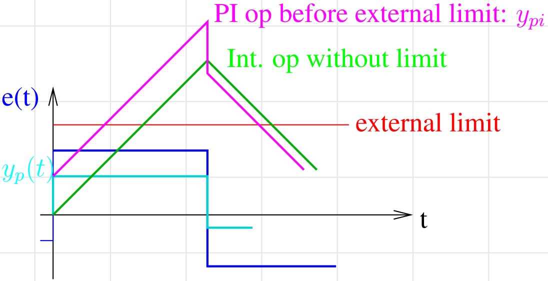

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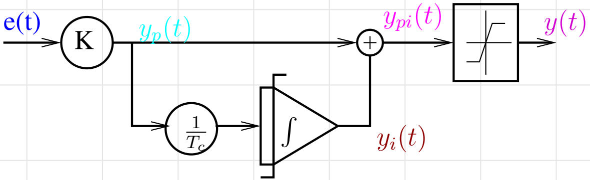

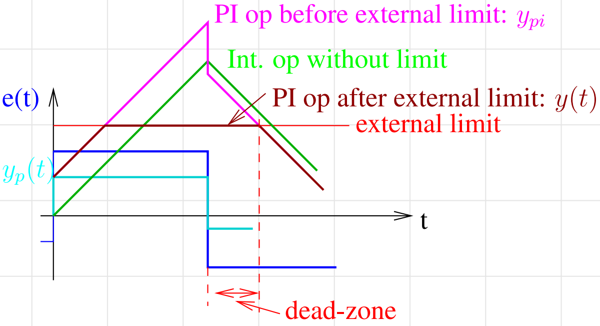

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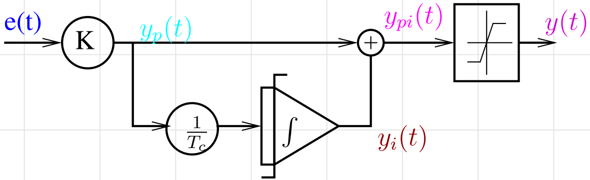

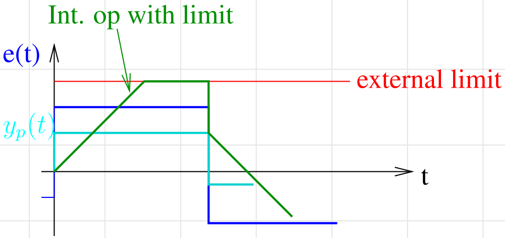

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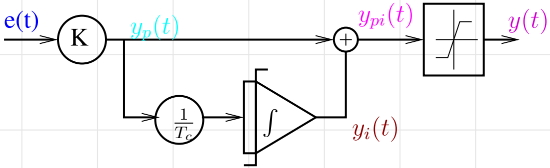
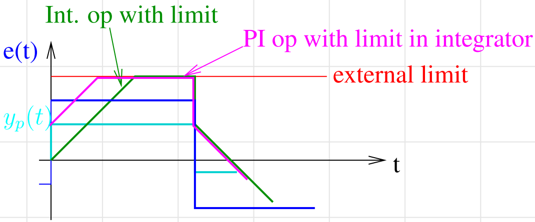
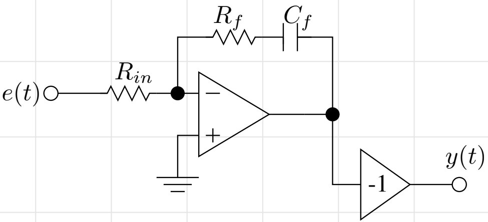




P-I Implementation

Analog



$$y(t) = \frac{R_f}{R_{in}} e\left(t\right) + \frac{1}{R_{in}C_f} \int e\left(t\right) dt$$

Digital

$$y(n) = Ke(n) + \frac{K}{T}\left[\frac{e(n)+e(n-1)}{2}\right] T_s + y(n-1)$$

PI Controller Transfer Function:

$$\frac{K(1+sT_c)}{sT_c}$$

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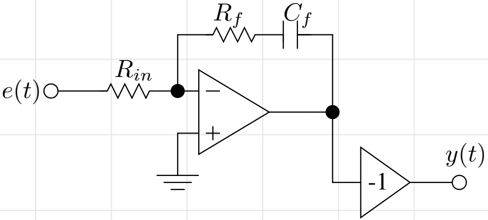

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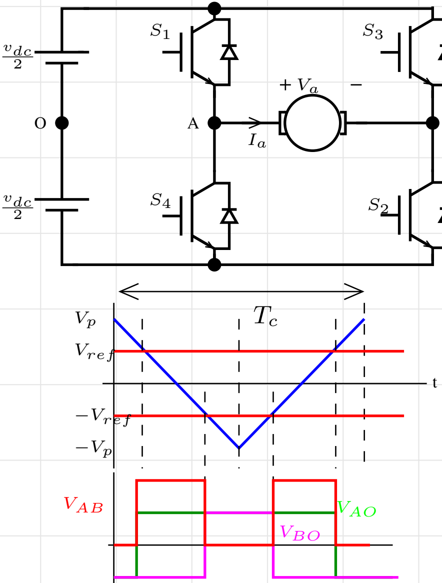
Converter Gain: Full Bridge



The switching law:

S_4 ON for$V_{tri} > V_{ref}$

S_1 ON for$V_{tri} < V_{ref}$

S_2 ON for$V_{tri} > -V_{ref}$

S_3 ON for$V_{tri} > -V_{ref}$

From the geometry, we see that:

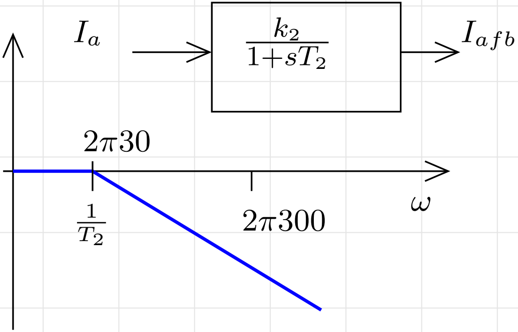
$$V_a = \frac{V_{dc}}{V_p} \cdot V_{ref}$$

$$\therefore$$

$$K_A = \frac{V_{DC}}{V_p}$$

The average delay, $T_d = \frac{T_c}{2}$

Current Sensor Transfer Function



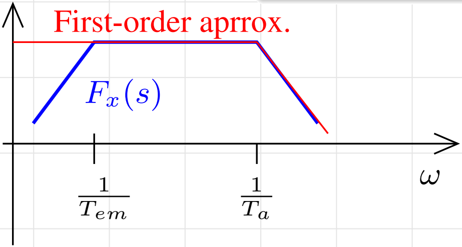
- Should respond to changes in I_a quickly
- Should reject switching frequency harmonics in the current
- For large f_s, the filter dynamics will not affect the drive response

Current Sensor Transfer Function

Let, $F_x(s) = \frac{1}{R_a} \cdot \frac{sT_{em}}{(1+sT_{em})(1+sT_a)}$

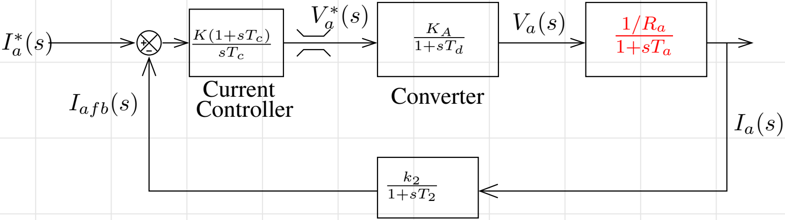
$= \frac{1}{R_a} \cdot \frac{sT_{em}}{1+s(T_{em}+T_a)+s^2 T_{em} T_a}$

For $T_a \ll T_{em}$, the above T.F will be same as the actual T.F for $\frac{I_a(s)}{V_a(s)}$.
i.e., $\frac{1}{R_a} \cdot \frac{sT_{em}}{sT_{em}(1+sT_a)+1}$



Current Loop

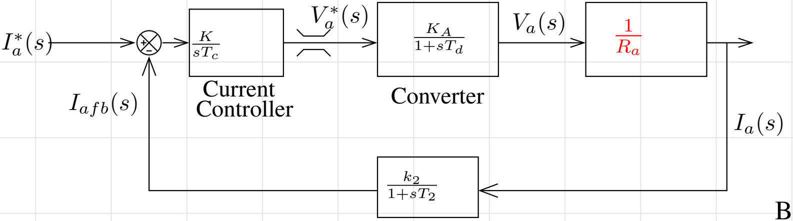
Current-loop simplified:



Where, $\sigma = T_d + T_2$

Current Loop

Current-loop simplified:



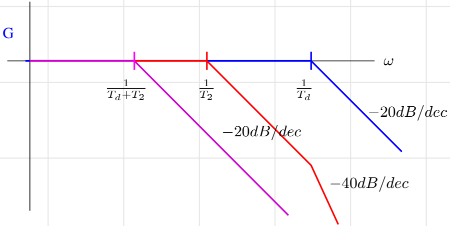
By choosing $T_c = T_a$. The resulting closed-loop T.F is a third-order one:

$$\frac{I_a(s)}{I_a^*(s)} = \frac{\frac{K_c K_A}{R_a}(1+sT_2)}{sT_c(1+sT_d)(1+sT_2) + \frac{K_c K_A k_2}{R_a}}$$

This can be approximated as:

$$\frac{I_a(s)}{I_a^*(s)} \approx \frac{\frac{K_c K_A}{R_a}(1+sT_2)}{sT_a(1+s\sigma) + \frac{K_c K_A k_2}{R_a}}$$

Current-loop



With $T_c = T_a$, the approximated characteristic equation is,

$$s^2 + s\frac{1}{\sigma} + \frac{K_c K_A k_2}{R_a T_a} \cdot \frac{1}{\sigma} k_2$$

comparing to the standard second-order T.F:

$$\begin{aligned} {\omega_n}^2 &= \frac{K_c K_A}{R_a T_a} \frac{1}{\sigma} \cdot k_2 \\ \zeta &= \frac{1}{\sigma} \frac{1}{2\omega_n} \end{aligned}$$

For $\zeta = 0.707$, we get:

$$K_c = \frac{R_a T_a}{k_2 K_A} \cdot \frac{1}{2\sigma}$$

Current-loop

With K_c chosen as above, the current-loop T.F becomes:

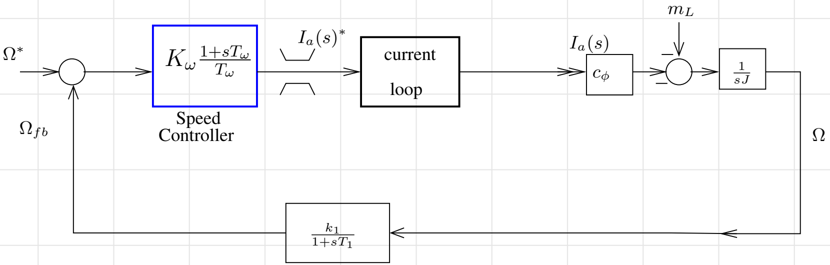
$$\frac{I_a(s)}{I_a^*(s)} \approx \frac{1}{k_2} \cdot \frac{(1+sT_2)}{2\sigma^2 s^2 + 2\sigma s + 1}$$

The zero $(1+sT_2)$ causes undesirable overshoot, and can be corrected by cancelling with a pole.

The current loop Band-width is:

$$BW \approx \frac{1}{2\sigma}$$

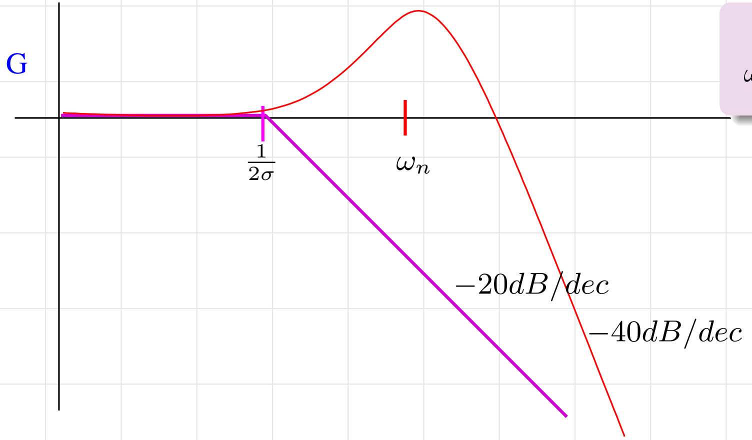
Speed-loop



The resulting T.F is a 5th order system. To proceed, we need to simplify and approximate. The current-loop T.F is further simplified as:

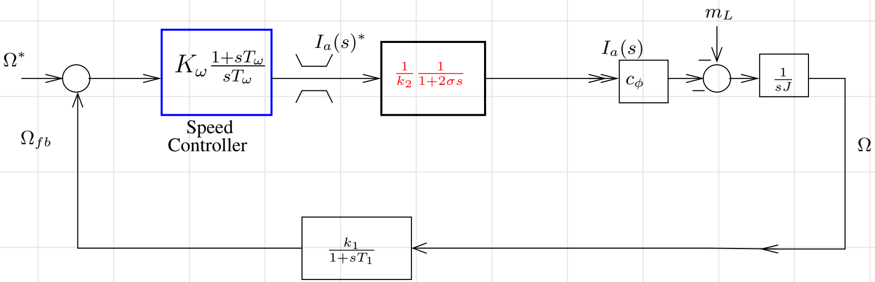
$$\frac{I_a(s)}{I_a^*(s)} \approx \frac{1}{k_2} \cdot \frac{(1+sT_2)}{2\sigma^2 s^2 + 2\sigma s + 1} \approx \frac{1}{k_2} \frac{1}{1+2\sigma s}$$

Speed-loop



$$\omega_n = \frac{1}{\sqrt{2}\sigma}$$

Speed-loop Design



We cannot follow the method used in current-loop design here, as the plant has an integrator.

Speed-loop Design

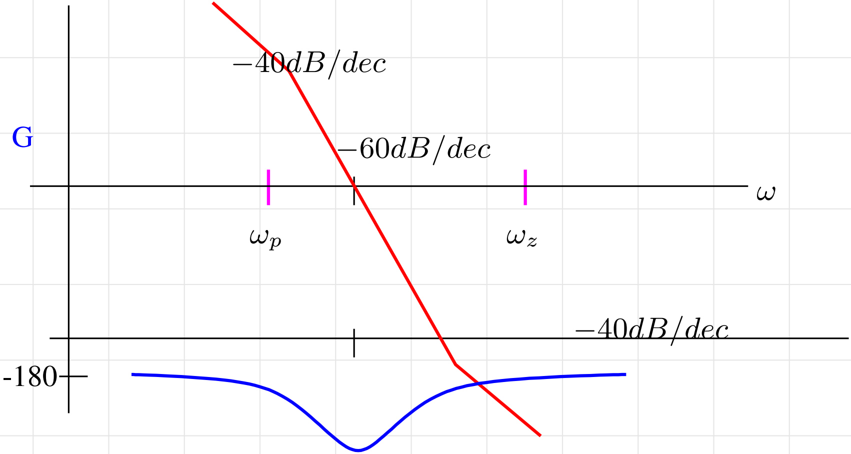
Symmetric Optimum method is used here.

$$G(s)H(s) = K_\omega \frac{1 + sT_\omega}{sT_\omega} \cdot \frac{1/k_2}{1 + 2\sigma s} \cdot \frac{c_\phi}{sJ} \cdot \frac{k_1}{1 + sT_1}$$

$$G(s)H(s) \approx K_\omega \frac{1 + sT_\omega}{sT_\omega} \cdot \frac{c_\phi}{k_2} \cdot \frac{1}{sJ} \cdot \frac{k_1}{1 + \delta s}$$

where, $\delta = 2\sigma + T_1$.

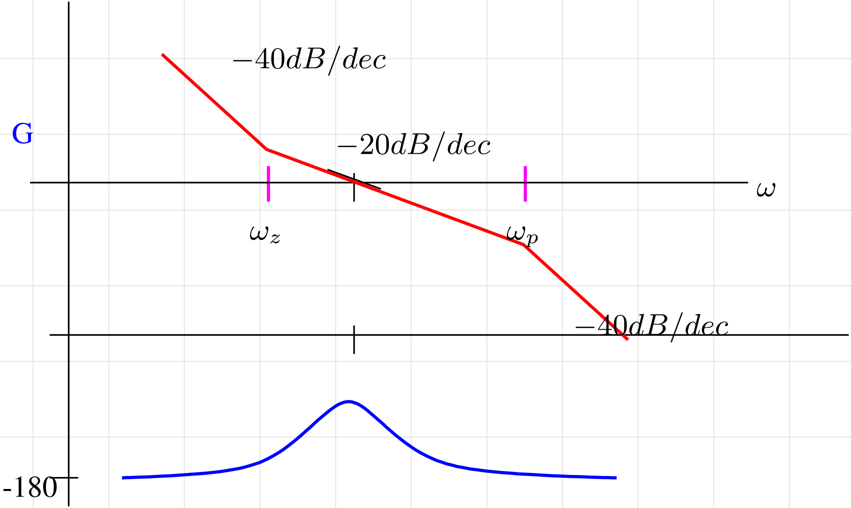
For $\omega_p < \omega_z$:



Phase margin is negative.

Speed-loop Design

Phase margin is negative. For $\omega_z < \omega_p$:



Placing the zero before the pole will improve the phase-margin.

Speed-loop Design

$$\omega_z = \frac{1}{T_\omega}$$

Choose the speed-contoller time-constant as:

$$T_\omega = a^2\delta, \quad \text{where } a > 1$$

Choose the cross-over frequency as the harmonic mean of the pole and zero frequencies.

$$\omega_c = \sqrt{\omega_z \omega_p}$$

$$|GH(j\omega)| = k_\omega \frac{\sqrt{1+(\omega T_\omega)^2}}{\omega T_\omega} \cdot \frac{1/k_2}{\sqrt{1+(\omega\delta)^2}} \cdot \frac{c_\phi}{J\omega} \cdot K_1$$

at $\omega = \omega_c$, $|GH(j\omega)| = 1$
(Gain-cross over frequency).

Or, $$|GH(j\omega)| = 1 = \frac{K_\omega \cdot c_\phi \cdot K_1}{k_2 J} \cdot a\delta$$

Which gives us,

Or, $$K_\omega = \frac{k_2 J}{c_\phi K_1 a\delta}$$ a=2 is an optimum value.

Speed-loop Design

The phase margin can be obtained as,

$$\text{Or,} \qquad \phi_M = \arctan(a) - \arctan\left(\frac{1}{a}\right)$$

Other considerations:

- Feed-forward of back emf
- Rate-of-change limiter for references

Digital Implementation: Fixed-point Vs Floating-Point

- Per-unit systems is adopted for fixed-point implementations
- A base value is chosen for all variables (voltage, frequency, phase, current etc)
- All variables are expressed in p.u
- p.u values are converted in to digital equivalents using fixed-point arithmetic
- Base conversion is done as per accuracy requirements

Digital Implementation: An example

- Let the input voltage be varying in the range $230V \pm 10\%$.
- The maximum voltage is then 357.742V
- If the base voltage is chosen as 360V, the maximum possible voltage is 0.9937 p.u

Digital Implementation: An example

In digital implementation, suppose we use a 12 bit ADC with an input voltage range $\pm 10V$.
The ADC will give digital equivalent values as follows:

ADC input voltage	12 bit Digital output	p.u for 5V base 5V base	p.u for 10V base 10 V base
+10 V	7FFh	2 p.u	1 p.u
+5 V	3FFh	1 p.u	0.5 p.u
+2.5 V	1FFh	0.5 p.u	0.25 p.u
+1.25 V	FFh	0.25 p.u	0.125 p.u
0 V	000h	0 p.u	0 p.u
-1.25 V	F01h	-0.25 p. u	-0.125 p.u
-2.5 V	E01h	-0.5 p.u	-0.25 p. u
-5.0 V	C01h	-1.0 p.u	-0.5 p.u
-10 V	801h	-2.0 p.u	-1.0 p.u

Digital Implementation: An Example

We may choose the input voltage-sensor in different ways.
For example:

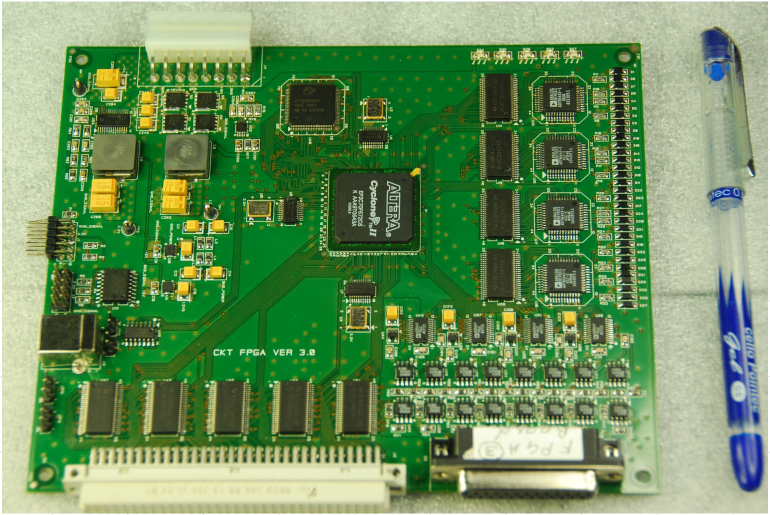
1. The nominal input voltage range of the ADC is $\pm 10V$ for the maximum expected input voltage
2. Leave enough room for the input voltage, and choose $\pm 5V$ as the nominal ADC input voltage range.

In the first case, we must choose the sensor-gain such that the ADC always get a voltage inside its range of $\pm 10V$.
In the second case, we must choose the sensor-gain in such a way that the ADC gets a nominal voltage of 5V when the input voltage is in the nominal range.
Here, however, we can have an unexpected higher voltage signal at the ADC input upto 2 p.u.
Normally, 2 p.u range is kept for signals like current, speed etc.

Some considerations

- Multiplication accuracy
  - Intermediate calculations should be done at higher base values
- Changing the base values
- Sampling frequency

FPGA based digital platform



FPGA platform: features

- 80 digital I/Os
- 16 Analog input channels (with 6.4 μs A/D conversion time per channel)
- 8 Analog output channels (with a DAC settling time of 80 ns)
- ALTERA EP2C70F672C8 FPGA with 68,416 logic elements
- USB and CAN transceiver interfaces
- On board SRAM (64K$\times$18)
- Three clocks at 20 MHz each
- JTAG interface

FPGA platform: Architecture

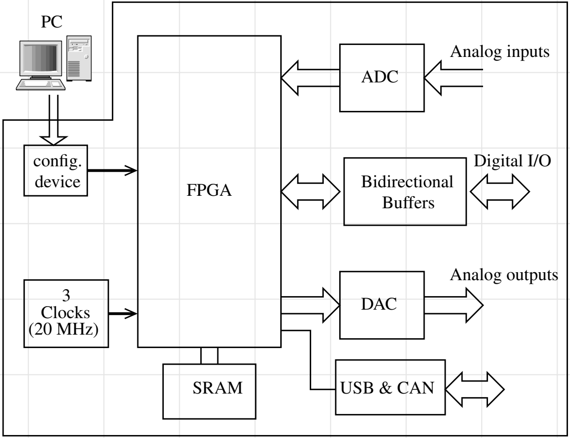


Figure: Block diagram of FPGA controller

References

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2. Werner Leonhard, ?Control of Electrical Drives,? Springer International, Third Ed, 2001

Thank You